Model 2008B Pulsed Optical Feedback Preamplifier

9231791C 4/02

User's Manual

Canberra Industries, 800 Research Parkway, Meriden, CT 06450
Tel: 203-238-2351 FAX: 203-235-1347 http://www.canberra.com

The information in this document describes the product as accurately as possible, but is subject to change without notice.

Printed in the United States of America.

Table of Contents

Notes

1. Introduction

There are different versions of the Model 2008 preamplifier in use on different detectors. Two of the most common types, the 2008B and 2008B ISA/DSA are described in this manual.

2. Model 2008B

The Canberra Model 2008B is a low-noise charge-sensitive preamplifier for use with cryogenically cooled Ge and Si radiation detectors. To minimize noise, the input FET is located near the detector element, where it is operated at low temperature. To further reduce noise, the feedback resistor has been eliminated and the charge integrator is discharged by an LED, which illuminates the FET, as required, to keep the amplifier from saturating.

For detectors equipped with a PRTD (Platinum Resistance Temperature Detector), the 2008B is equipped with a warm-up sensor/high voltage inhibit circuit. This circuit is used to disable the High Voltage Power Supply in case of accidental detector warm-up. Warm-up with bias applied to a detector can lead to FET damage.

Circuit Description

Refer to the block diagram (Figure 1) and to schematic diagram B-31866.

Charge Sensitive Preamplifier

The 2008B includes a H.V. filter network comprising two RC Filter Stages (R24-C11 and R25-C12). The test input is coupled into the preamplifier through the capacitance of the detector element by means of a signal imposed on the (not quite) ground side of the second filter capacitor.

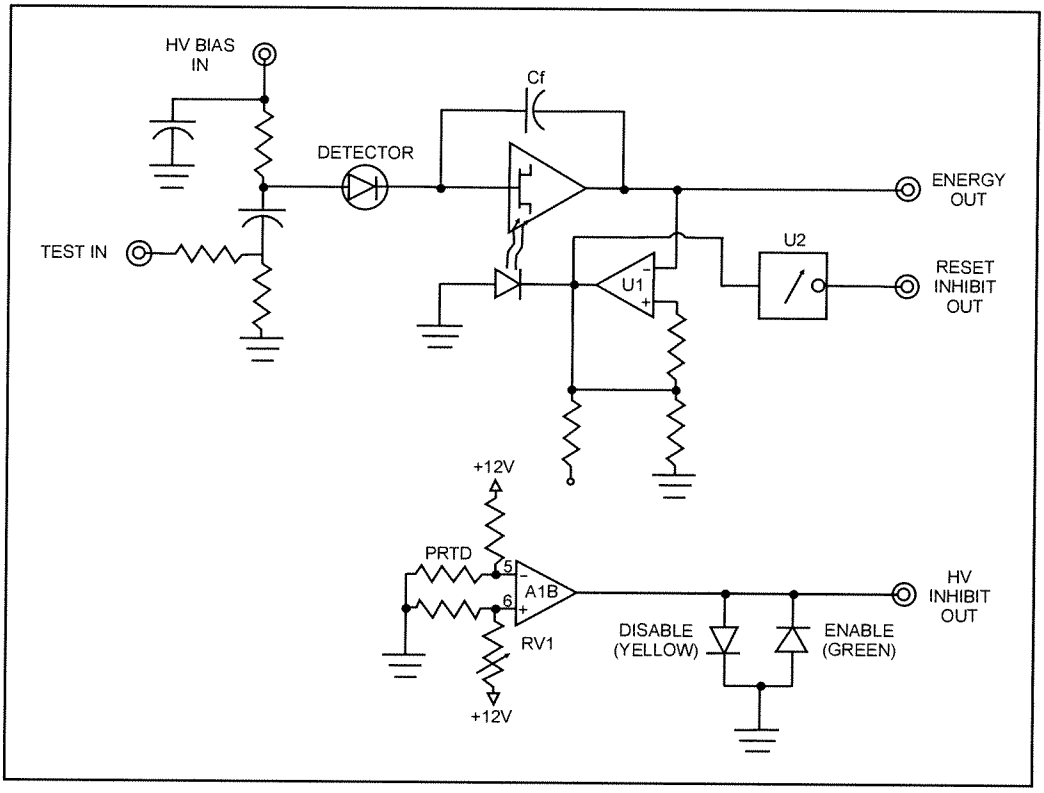

Figure 1 2008B Block Diagram

The input FET is located in the detector chamber, where it is cooled to an optimum temperature. The LED is optically coupled to the FET. On cryostats so equipped, the PRTD is located on or near the detector holder.

The charge sensitive stage is an operational amplifier operating with capacitive feedback that makes it charge sensitive. The transfer function for the preamplifier is:

$$V_o = \frac{Q_i}{C_f}$$

Where

V_o = Voltage out
Q_i = Charge in
C_f = Feedback capacitance

Comparator/Reset Circuit

Each photon interaction in the detector liberates a quantity of charge, which results in a voltage step at the preamplifier output.

These steps produce a random staircase output, which if left unchecked, would drive the preamplifier into saturation. To keep the preamplifier in its normal operating range, a comparator-driven LED illuminates the FET and discharges the integrator before it reaches its operational limit.

The comparator (U1) is biased to fire the LED (through driver Q6) when the output voltage reaches approximately 0 volts. It resets when the output returns to approximately –4 volts. Thus in normal operation the output voltage range of the preamplifier is about –4 to 0 volts. The ramp rate (reset rate) depends on the detector leakage current and on the energy rate deposited in the detector element.

Reset Inhibit Circuit

When the preamplifier resets, the output swings (negatively) by about 4 volts in a few microseconds. This represents a large overload signal to the associated shaping amplifier, which goes dead for several pulse widths. This, in addition to spurious effects of light on the FET, results in dead time, as well as distorted signals.

To correct for dead time loss and to prevent analysis of distorted signals, the 2008B is equipped with a monostable multivibrator (one-shot), which produces a TTL gating signal that can be used to gate off an ADC to prevent analysis of distorted or spurious signals. When used with Canberra's signal processing electronics, this signal goes into the inhibit input for both rejection and live time correction.

The output pulse width is adjustable by means of RV3 (a rear panel control on box-style preamps or an internal control on slimline preamps).

Warm-up Sensor /H.V. Inhibit Circuit

Refer to the LN_2 Monitor Board's schematic diagram, B-26892.

This circuit monitors the internal temperature on detectors which are equipped with a PRTD (Platinum Resistance Temperature Detector) and provides a signal to inhibit the H.V. Bias Supply in case warm-up begins with the H.V. on. This protects the FET from the arcing that can take place when cryostat pressure rises as the adsorber, which maintains vacuum, warms up and releases gas. The potential for arcing is not great with the small Ge and Si detectors used with the 2008B because they usually operate with relatively low bias voltage.

Comparator A1B is factory adjusted by means of RV1 with a 50 mV margin between normal (cold) temperature and the trigger point. If this circuit triggers when the detector is cold and with an adequate LN_2 level, it may be due to a loss of vacuum and a consequent rise in internal temperature. Check the LN_2 loss rate and for other signs of poor vacuum before readjusting RV1.

RV1 Adjustment

If there are no signs of vacuum failure readjust as follows: With the H.V. off, measure the voltage between pins 5 and 6 on comparator A1B. Adjust RV1 until the yellow LED comes on, then turn RVl in the opposite direction until the green LED comes on. Continue until the voltage between pins 5 and 6 is 50 mV.

Jumpers

Wire jumper W3 on the board can be used to connect the PRTD to a Test Point instead of to the circuit.

Wire jumper W4 at the output, when installed, provides an enable signal of + 5 V dc (TTL). The normal enable signal level is + 12 V dc. In both cases the disable signal level is 0.5 V dc.

Note: The auxiliary (piggyback) PC board containing the HV Inhibit Circuit also contains a circuit which drives an overload indicator. This circuit is used only with RC Feedback preamplifiers.

3. Models 2008B-ISA and 2008B-DSA

The Canberra Models 2008B-ISA and 2008B-DSA are low-noise charge-sensitive preamplifiers for use with cryogenically cooled Ge and Si radiation detectors. To minimize noise the input FET is located near the detector element where it is operated at low temperature. To further reduce noise, the feedback resistor has been eliminated and the charge integrator is discharged by an LED, which illuminates the FET as required to keep the amplifier from saturating.

Both the 2008B-ISA and the 2008B-DSA are wired to accept an auxiliary circuit board supplied by the customer. This circuit includes ±12 V regulators which allow the preamplifier to operate from 24 V power supplies. It also contains a circuit that reads the internal Platinum Resistance Temperature Detector (PRTD) and provides a H.V. inhibit signal to the associated H.V. Bias Supply.

Circuit Description

Refer to the block diagram (Figure 2) and to schematic diagram B-31866.

Charge Sensitive Preamplifier

The input FET is located in the detector chamber where it is cooled to an optimum temperature. The LED is optically coupled to the FET. On cryostats so equipped, the PRTD is located on or near the detector holder.

The charge sensitive stage is an operational amplifier operating with capacitive feedback that makes it charge sensitive. The transfer function for the preamplifier is:

$$V_o = \frac{Q_i}{C_f}$$

Where

V_o = Voltage out
Q_i = Charge in
C_f = Feedback capacitance

Gain adjustment is achieved by selection of resistor R13 which forms a feedback voltage divider in conjunction with R14.

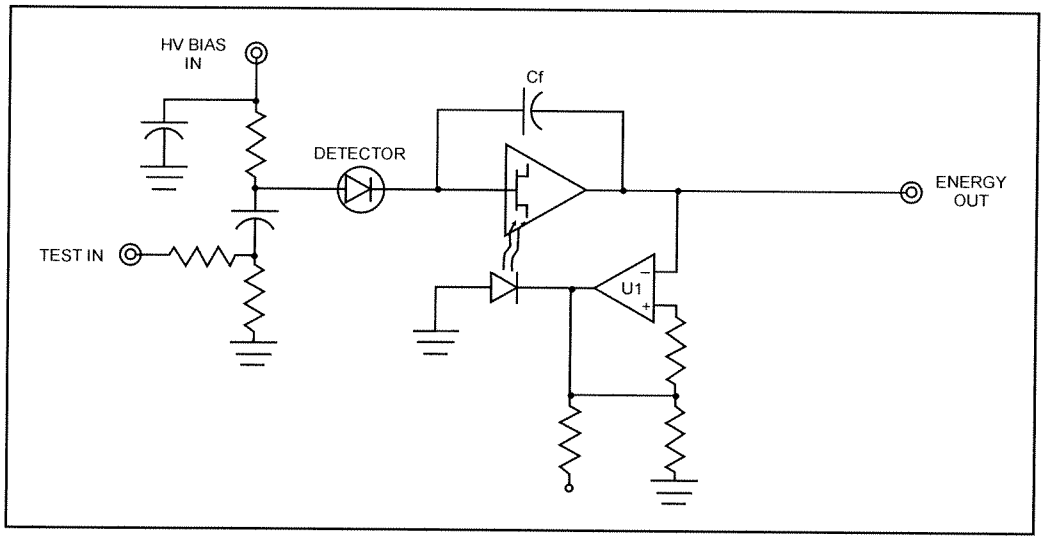

Figure 2 2008B-ISA/DSA Block Diagram

Comparator/Reset Circuit

Each photon interaction in the detector liberates a quantity of charge which results in a voltage step at the preamplifier output. These steps produce a random staircase output, which if left unchecked, would drive the preamplifier into saturation. To keep the preamplifier in its normal operating range, a comparator-driven LED illuminates the FET and discharges the integrator before it reaches its operational limit.

The comparator (U1) is biased to fire the LED (through driver Q6) when the output voltage reaches approximately 0 volts. It resets when the output returns to approximately – 4 volts. Thus in normal operation the output voltage range of the preamplifier is about – 4 to 0 volts. The ramp rate (reset rate) depends on the detector leakage current and on the rate energy is deposited in the detector.

Wiring for Auxiliary Circuit

Refer to the Interconnect Wiring and H.V. Filter's schematic diagram, B-33349.

The customer-supplied auxiliary board attaches to the preamplifier rail and is connected to the main PC board by means of a pigtail cable. The H.V. Filter Assembly (potted in the case of the 2008B-ISA only) is also shown on this schematic diagram. This diagram also shows the LN Monitor Input (BNC Connector) which is routed out on pin 8 of the 9-pin D power connector.

Preamplifier Power

Refer to the preamplifier's schematic diagram, B-31866. When the (customer supplied) Auxiliary Board is used, jumpers JP2 and JP3 *must be removed*. In this case ±12 V is supplied from the auxiliary board.

WARNING If jumpers JP2 and JP3 are installed when the auxiliary board is present, the outputs of the two 12 V supplies will be connected. This is likely to cause circuit failure.

Reset Inhibit Circuit

The Reset Inhibit circuit, which provides a gating signal to disable data acquisition during and following reset, is not used in the ISA and DSA versions of the 2008B. The Inhibit Output connector is not provided.

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES OR REMEDIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, EXEMPLARY, PUNITIVE, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE. REPAIR OR REPLACEMENT OF THE SOFTWARE OR EQUIPMENT DURING THE APPLICABLE WARRANTY PERIOD AT CANBERRA'S COST, OR, IN THE CASE OF DEFECTIVE SERVICES, REPERFORMANCE AT CANBERRA'S COST, IS YOUR SOLE AND EXCLUSIVE REMEDY UNDER THIS WARRANTY.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

Software License

When purchasing our software, you have purchased a license to use the software, not the software itself. Because title to the software remains with us, you may not sell, distribute or otherwise transfer the software. This license allows you to use the software on only one computer at a time. You must get our written permission for any exception to this limited license.

BACKUP COPIES

Our software is protected by United States Copyright Law and by International Copyright Treaties. You have our express permission to make one archival copy of the software for backup protection. You may not copy our software or any part of it for any other purpose.