TRIUMF

RTRIG

● ACC
● ETRIG
● REV

○ REV TRIG IN

○ ○ EXTRACT TRIG 1

○ ○ EXTRACT TRIG 2

ISAC KICKER TRIG

YCB3N TRIG

YCB3S TRIG
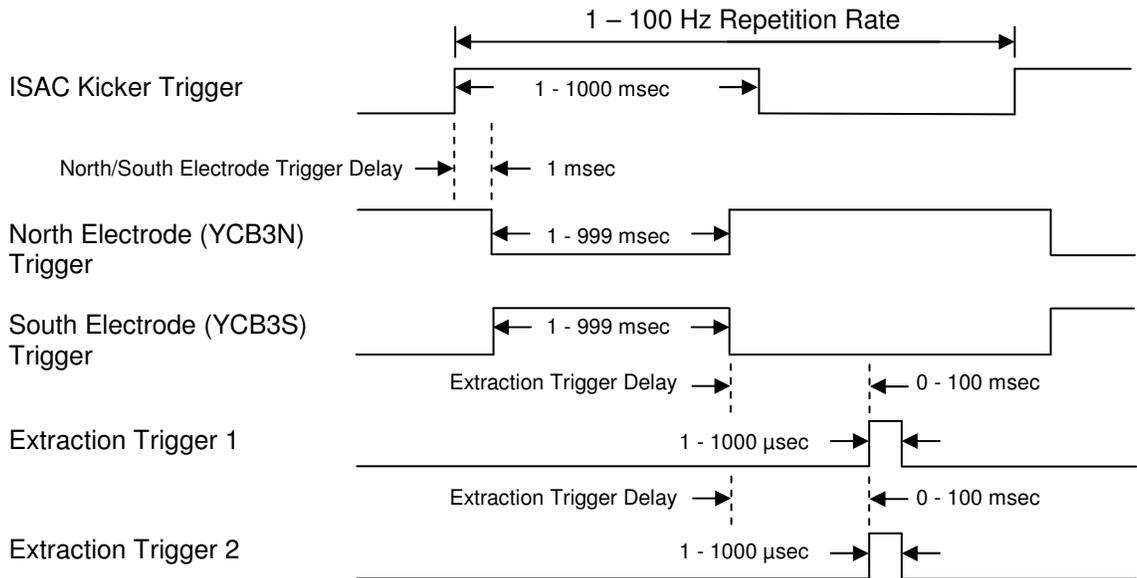
EXTRACT TRIG 1

EXTRACT TRIG 2

REVERSE TRIGGER ONLY

TITAN VME Reverse Trigger Module

General Description

The VME Reverse Trigger Module (RTRIG) was designed to generate the following gate pulses.

Reverse Extraction

1 – 100 Hz Repetition Rate

ISAC Kicker Trigger   1 - 1000 msec

North/South Electrode Trigger Delay →   ← 1 msec

North Electrode (YCB3N) Trigger   1 - 999 msec

South Electrode (YCB3S) Trigger   1 - 999 msec

Extraction Trigger Delay →   ← 0 - 100 msec

Extraction Trigger 1   1 - 1000 µsec →

Extraction Trigger Delay →   ← 0 - 100 msec

Extraction Trigger 2   1 - 1000 µsec →

Once the RTRIG module detects a trigger pulse, the waveforms as described above will be generated. If a second main trigger pulse is injected before the **ISAC kicker trigger** pulse finishes, it is ignored.

VME Interface   SLAVE – A16, D16, D8 (OE)

The RTRIG requires a 16-bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The RTRIG will only respond to A16 address cycles.
Short Supervisory & short nonprivileged access - 0x2D, 0x29

Base Address Selection

Each jumper corresponds to address bits A15 – A6 on the VME address bus. Installing a jumper for each address bit will select a 0 (low) for the corresponding VME address bit.

Table 1 Base Address Selection

Jumpers Installed (X)										Address Range
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	
X	X	X	X	X	X	X	X	X	X	0000 – 003F
-	X	X	X	X	X	X	X	X	X	**8000 – 803F**
-	-	X	X	X	X	X	X	X	X	C000 – C03F
-	-	-	X	X	X	X	X	X	X	E000 – E03F
-	-	-	-	X	X	X	X	X	X	F000 – F03F
-	-	-	-	-	X	X	X	X	X	F800 – F83F
-	-	-	-	-	-	X	X	X	X	FC00 – FC3F

Input Description

The reverse main trigger input accept TTL levels and are 50Ω terminated.

Output (Non-Fibre) Description

All outputs have TTL levels with 50 Ω drive capability. The dual non-fibre outputs are for the **extraction trigger 1 & 2** signals.

With an active signal, each TTL output can be set to output +5V or 0V.

Output (Fibre) Description

The first fibre optic output is for the **ISAC kicker trigger**. The following four fibre outputs are for the **north electrode (YCB3N) trigger**, the **south electrode (YCB3S) trigger,** the **extraction trigger 1** and the **extraction trigger 2** signals.
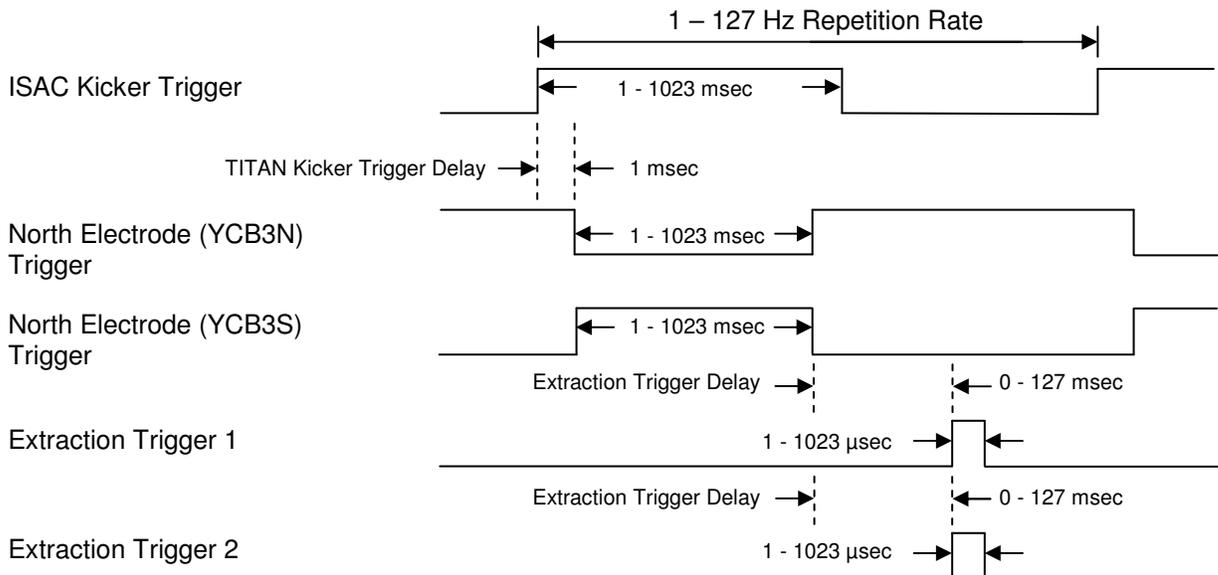
With an active signal, each fibre output can be set to output light or stay dark.

Table 2 Default Register Values

Address (HEX)	Reset Value (HEX)	Operation	Description	Size
3F 10	00	R	RESERVED	8 bits
0F	00	R/W	Module Register Reset to Default	0 bits
0E	00	R	**Reserved**	8 bits
0D	00	R	**Reserved**	8 bits
0C	00	R	**Reserved**	8 bits
0B	00	R/W	Output Inversion	5 bits
0A	00	R/W	Internal/External Trigger Select	1 bits
09	00	R/W	Extraction Trigger Enable	1 bits
08	01	R/W	Internal Trigger Repetition Rate	7 bits
06	0001	R/W	Extraction trigger width	10 bits
05	00	R/W	Extraction trigger delay	7 bits
04	00	R	**Reserved**	8 bits
02	0001	R/W	North/south electrode trigger width	10 bits
00	0001	R/W	ISAC kicker trigger width	10 bits

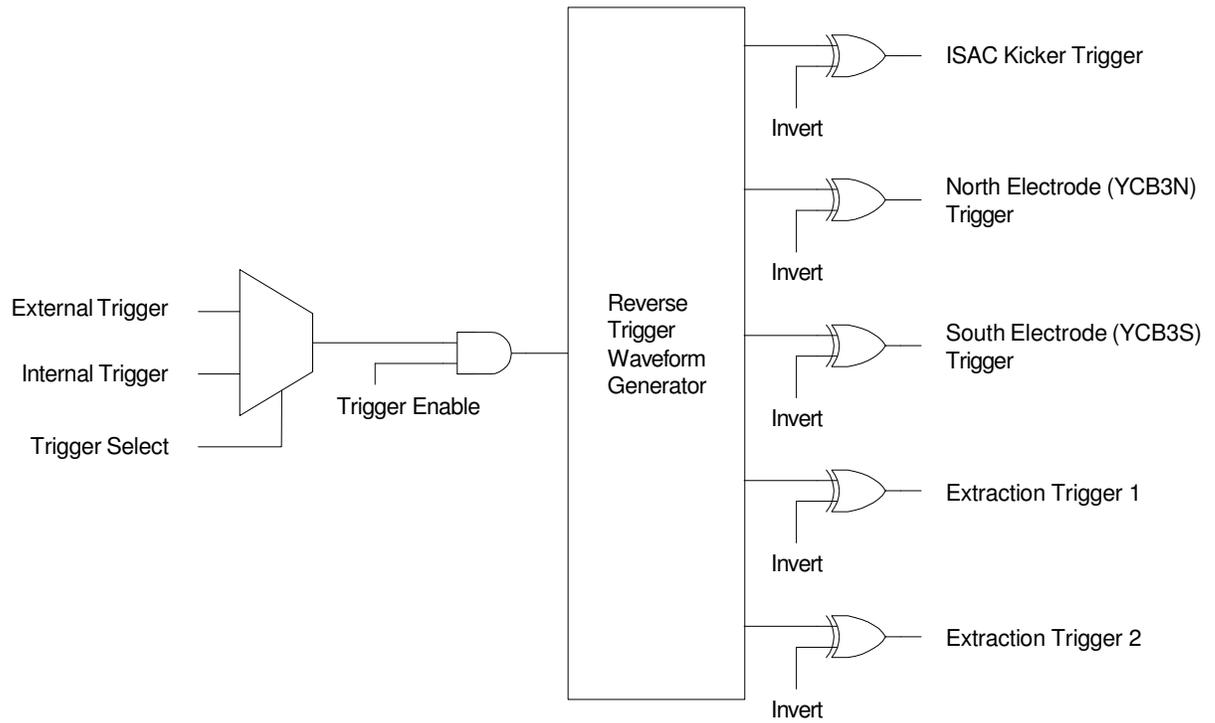# Output Waveforms Minimum and Maximum Settings

Reverse Extraction

Functional Block Diagrams

Diagram 1 Reverse Extraction

External Trigger

Internal Trigger

Trigger Select

Trigger Enable

Reverse Trigger Waveform Generator

Invert — ISAC Kicker Trigger

Invert — North Electrode (YCB3N) Trigger

Invert — South Electrode (YCB3S) Trigger

Invert — Extraction Trigger 1

Invert — Extraction Trigger 2

Reverse Extraction Registers

ISAC Kicker Trigger Width

These registers will respond to a byte or a word access.

ADR	\$xxxxxx00 - 01															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R						R/W									
RESET	0						1									

width = register value x 1 ms

Minimum width   =   1 ms
Maximum width   =   1023 ms

By default, width is 1 ms.

North/South Electrode Trigger Width

These registers will respond to a byte or a word access.

ADR	\$xxxxxx02 - 03															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R						R/W									
RESET	0						1									

width = register value x 1 ms

Minimum width   =   1 ms
Maximum width   =   1023 ms

By default, width is 1 ms. The TITAN Kicker trigger is delayed 1 ms from the start of the ISAC Kicker trigger.

Extraction Trigger Delay

This register will respond to a byte or a word access.

ADR	\$xxxxxx05							
BIT	7	6	5	4	3	2	1	0
OPER	R	R/W						
RESET	0	0						

delay = register value x 1 ms

Minimum delay   =   0 ms
Maximum delay   =   127 ms

By default, delay is 0 ms. Extraction delay starts after the TITAN Kicker trigger has completed.

Extraction Trigger Width

These registers will respond to a byte or a word access.

ADR	$xxxxxx06 - 07															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R						R/W									
RESET	0						1									

width = register value x 1 µs

Minimum width   =   1 µs
Maximum width   =   1023 µs

By default, width is 1 µs.

Module Control Registers

Internal Trigger Repetition Rate

This register will respond to a byte or a word access.

ADR	$xxxxxx08							
BIT	7	6	5	4	3	2	1	0
OPER	R	R/W						
RESET	0	1						

repetition rate = register value x 1 Hz

Minimum repetition rate   =   1 Hz
Maximum repetition rate   =   127 Hz

By default, repetition rate is 1 Hz.

Extraction Trigger Enable

This register will respond to a byte or a word access.

ADR	$xxxxxx09							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

Bit 0:   0:   Reverse Extraction Disabled.
              1:    Enabled.

The enable signal applies to both internal and external triggers.

Internal/External Trigger Select

This register will respond to a byte or a word access.

ADR	$xxxxxx0A							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

Bit 0: 0: **Internal** trigger used.
             1: **External** trigger used.

Output Inversion

This register will respond to a byte or a word access.

ADR	$xxxxxx0B							
BIT	7	6	5	4	3	2	1	0
OPER	R			R/W	R/W	R/W	R/W	R/W
RESET	0			0	0	0	0	0

Bit 0: 0: ISAC Kicker – Normal Output.
             1: ISAC Kicker – Inverted Output.

Bit 1: 0: North Electrode (YCB3N) Trigger – Normal Output.
             1: North Electrode (YCB3N) Trigger – Inverted Output.

Bit 2: 0: South Electrode (YCB3S) Trigger – Normal Output.
             1: South Electrode (YCB3S) Trigger – Inverted Output.

Bit 3: 0: Extract 1 – Normal Output.
             1: Extract 1 – Inverted Output.

Bit 4: 0: Extract 2 – Normal Output.
             1: Extract 2 – Inverted Output.

Note: for fibres outputs
        normal output = fibre has light when signal is active.
        Inverted output = fibre is dark when signal is active.

        for TTL outputs
        normal output = +3V to +5V when signal is active.
        Inverted output = 0V when signal is active.

VME Reset Control

This register will respond to a byte or a word access.

ADR	$xxxxxx0F							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will reset all VME registers to default values.