FTRIG

● ACC
● ETRIG
● FWD

FWD TRIG IN

EXTRACT TRIG

DRIFT TUBE TRIG

EXTRACT TRIG

YCB3N TRIG

YCB3S TRIG

DRIFT TUBE TRIG

CAMERA TRIG

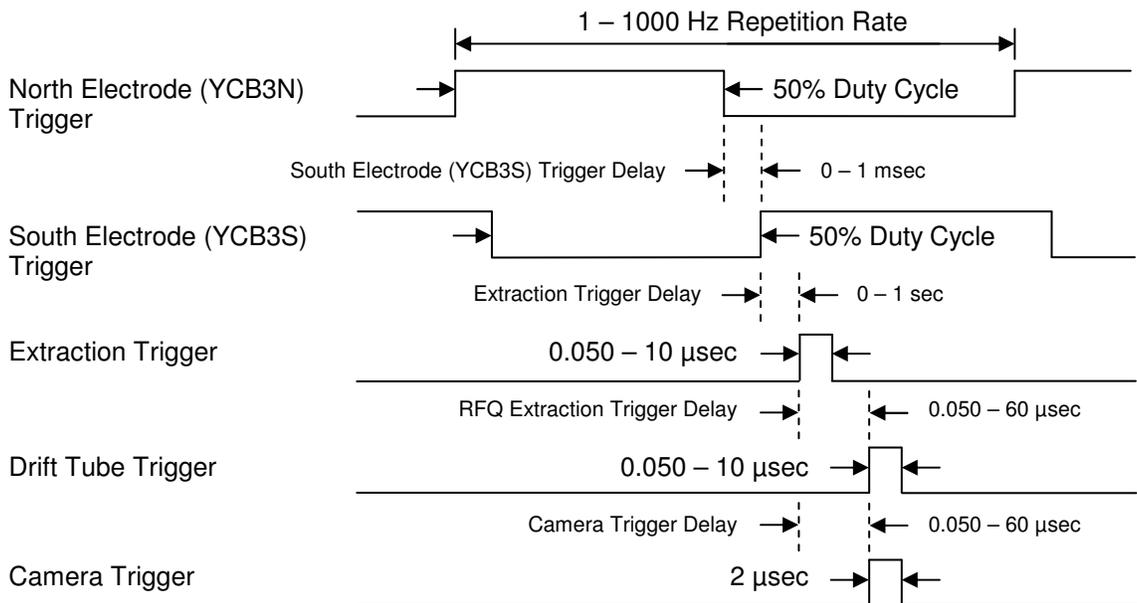FORWARD TRIGGER ONLY

TRIUMF

TITAN VME Forward Trigger Module

General Description

The VME Forward Trigger Module (FTRIG) was designed to generate the following gate pulses.

Forward Extraction

Once the FTRIG module detects a trigger pulse, the waveforms as described above will be generated. If a second main trigger pulse is injected before the **north electrode (YCB3N) trigger** pulse finishes, it is ignored. In external trigger mode, the **north electrode (YCB3N) trigger** and **south electrode (YCB3S) trigger** outputs are disabled and the south electrode (YCB3S) and extraction trigger delays are set to zero.

VME Interface   SLAVE – A16, D16, D8 (OE)

The FTRIG requires a 16-bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The FTRIG will only respond to A16 address cycles.
Short Supervisory & short nonprivileged access - 0x2D, 0x29

Base Address Selection

Each jumper corresponds to address bits A15 – A6 on the VME address bus. Installing a jumper for each address bit will select a 0 (low) for the corresponding VME address bit.

Table 1 Base Address Selection

Jumpers Installed (X)										Address Range
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	
X	X	X	X	X	X	X	X	X	X	0000 – 003F
-	X	X	X	X	X	X	X	X	X	*8000 – 803F*
-	-	X	X	X	X	X	X	X	X	C000 – C03F
-	-	-	X	X	X	X	X	X	X	E000 – E03F
-	-	-	-	X	X	X	X	X	X	F000 – F03F
-	-	-	-	-	X	X	X	X	X	F800 – F83F
-	-	-	-	-	-	X	X	X	X	FC00 – FC3F

Input Description

The forward main trigger input accept TTL levels and are 50Ω terminated.

Output (Non-Fibre) Description

All outputs have TTL levels with 50 Ω drive capability. The dual non-fibre outputs are for the **extraction triggers** and **drift tube triggers**.

Output (Fibre) Description

The first fibre optic output is for the **extraction trigger**. The following four fibre outputs are for the **north electrode (YCB3N) trigger**, the **south electrode (YCB3S) trigger, camera trigger** and the **drift tube trigger**.
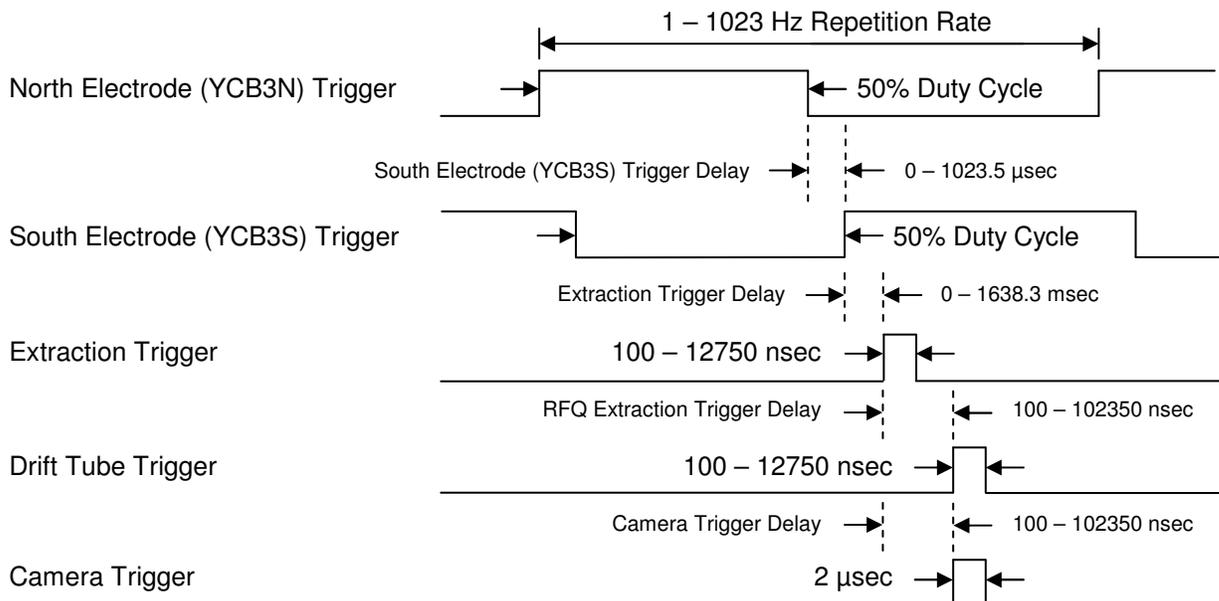
With an active signal, each fibre output can be set to output light or stay dark.

Table 2 Default Register Values

Address (HEX)	Reset Value (HEX)	Operation	Description	Size
3F 10	00	R	RESERVED	8 bits
0F	00	R/W	Module Register Reset to Default	0 bits
0E	00	R/W	Fibre Output Inversion	5 bits
0D	00	R/W	Internal/External Trigger Select	1 bits
0C	00	R/W	Extraction Trigger Enable	1 bits
0A	0001	R/W	Internal Trigger Repetition Rate	10 bits
08	0002	R/W	Camera trigger delay	11 bits
06	0002	R/W	Drift tube trigger delay	11 bits
05	02	R/W	Drift tube trigger width	8 bits
04	02	R/W	Extraction trigger width	8 bits
02	0001	R/W	Extraction trigger delay	14 bits
00	0000	R/W	South electrode (YCB3S) delay	11 bits

Output Waveforms Minimum and Maximum Settings

Forward Extraction

Functional Block Diagrams

Diagram 1 Forward Extraction

External Trigger

Internal Trigger

Trigger Select

Trigger Enable

Reverse
Trigger
Waveform
Generator

Invert

North Electrode (YCB3N)
Trigger

Invert

South Electrode (YCB3S)
Trigger

Invert

Extraction Trigger (Inversion
on Fibre Output Only)

Invert

Drift Tube Trigger

Invert

Camera Trigger
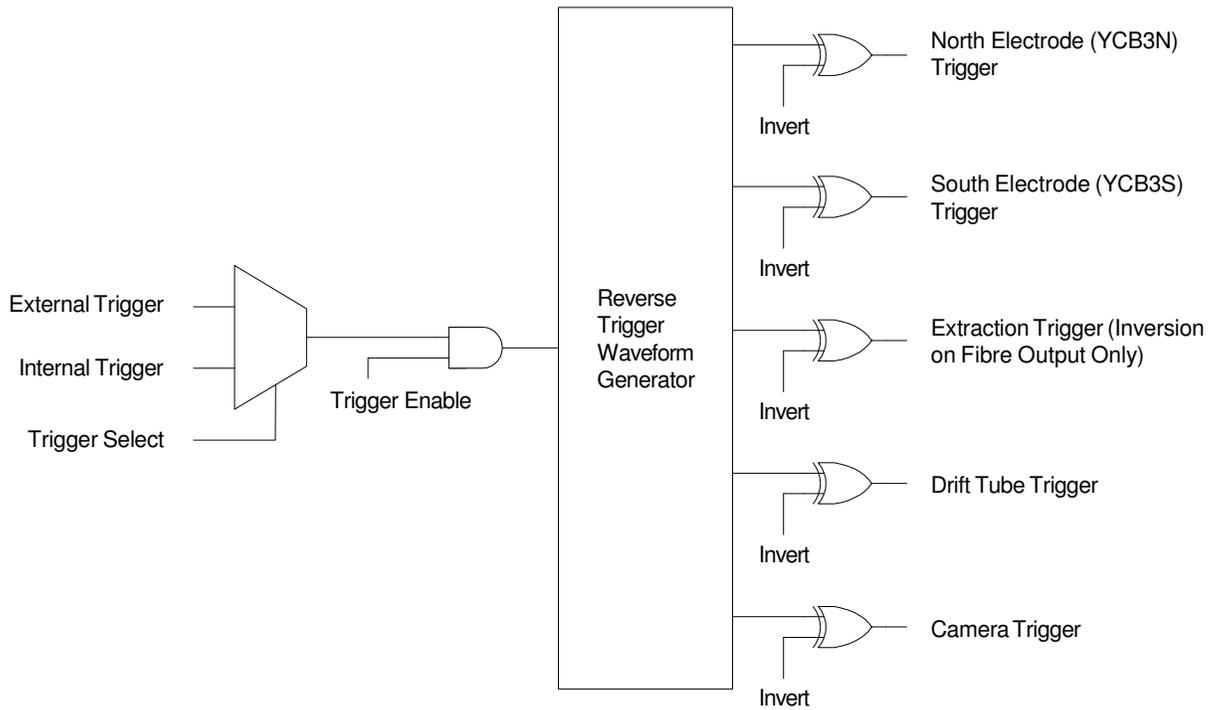
Forward Extraction Registers

South Electrode (YCB3S) Trigger Delay

These registers will respond to a byte or a word access.

ADR	$xxxxxx00 - 01															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R					R/W										
RESET	0					0										

delay = register value x 0.5 µs

Minimum delay   =   0 µs
Maximum delay   =   1023.5 µs

By default, delay is 0 µs. When using external triggering, the south electrode (YCB3S) and the north electrode (YCB3N) outputs are disabled.

Extraction Trigger Delay

These registers will respond to a byte or a word access.

ADR	$xxxxxx02 - 03															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R	R/W														
RESET	0	1														

delay = register value x 0.1 ms

Minimum delay   =   0.1 ms
Maximum delay   =   1638.3 ms

By default, delay is 0.1 ms. When using external triggering, the extraction trigger delay is set to zero no matter what value is in the extraction trigger delay register. Value in register **MUST** be greater than or equal to 1.

Extraction Trigger Width

These registers will respond to a byte or a word access.

ADR	$xxxxxx04							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	2							

width = register value x 50 ns

Minimum width   =   100 ns
Maximum width   =   12.75 µs

By default, width is 100 ns. Value in register **MUST** be greater than or equal to 2.

Drift Tube Trigger Width

These registers will respond to a byte or a word access.

ADR	$xxxxxx05							
BIT	7	6	5	4	3	2	1	0
OPER	R/W							
RESET	2							

width = register value x 50 ns

Minimum width = 100 ns
Maximum width = 12.75 µs

By default, width is 100 ns. Value in register **MUST** be greater than or equal to 2.

Drift Tube Trigger Delay

These registers will respond to a byte or a word access.

ADR	$xxxxxx06 - 07															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				2											

delay = register value x 50 ns

Minimum delay = 100 ns
Maximum delay = 102.35 µs

By default, delay is 100 ns. Value in register **MUST** be greater than or equal to 2.

Camera Trigger Delay

These registers will respond to a byte or a word access.

ADR	$xxxxxx08 - 09															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R				R/W											
RESET	0				2											

delay = register value x 50 ns

Minimum delay = 100 ns
Maximum delay = 102.35 µs

By default, delay is 100 ns. Value in register **MUST** be greater than or equal to 2. The camera trigger pulse width is fixed at 2 µs.

Module Control Registers

Internal Trigger Repetition Rate

This register will respond to a byte or a word access.

ADR	$xxxxxx0A – 0B															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPER	R						R/W									
RESET	0						1									

repetition rate = register value x 1 Hz

Minimum repetition rate = 1 Hz
Maximum repetition rate = 1023 Hz

By default, repetition rate is 1 Hz. Value in register **MUST** be greater than or equal to 1.

Extraction Trigger Enable

These registers will respond to a byte or a word access.

ADR	$xxxxxx0C							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

Bit 0: 0: Forward Extraction Disabled.
        1: Enabled.

The enable signal applies to both internal and external triggers.

Internal/External Trigger Select

This register will respond to a byte or a word access.

ADR	$xxxxxx0D							
BIT	7	6	5	4	3	2	1	0
OPER	R							R/W
RESET	0							0

Bit 0: 0: **Internal** trigger used.
        1: **External** trigger used.

Fibre Output Inversion

This register will respond to a byte or a word access.

ADR	\$xxxxxx0E							
BIT	7	6	5	4	3	2	1	0
OPER	R			R/W	R/W	R/W	R/W	R/W
RESET	0			0	0	0	0	0

Bit 0: 0: Extraction trigger – Normal Output.
  1: Extraction trigger – Inverted Output.

Bit 1: 0: North electrode (YCB3N) trigger – Normal Output.
  1: North electrode (YCB3N) trigger – Inverted Output.

Bit 2: 0: South electrode (YCB3S) trigger – Normal Output.
  1: South electrode (YCB3S) trigger – Inverted Output.

Bit 3: 0: Drift trigger – Normal Output.
  1: Drift trigger – Inverted Output.

Bit 4: 0: Camera trigger – Normal Output.
  1: Camera trigger – Inverted Output.

Note: normal output = fibre has light when signal is active.
  Inverted output = fibre is dark when signal is active.

VME Reset Control

This register will respond to a byte or a word access.

ADR	\$xxxxxx0F							
BIT	7	6	5	4	3	2	1	0
OPER	R							
RESET	0							

Write cycle will reset all VME registers to default values.