DEVELOPMENT OF A HIGH-VOLTAGE 3 MHZ RF-DC COUPLING BOARD

by

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Submitted to

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PREFACE

This report is presented as a fulfillment of the work term requirements at the University of British Columbia and as a reference for further development of the TITAN's RFQ ion beam cooler and buncher.

During my work term with the TRIUMF's TITAN group, I designed, modified, and tested a single-polarity high-voltage RF prototype driver for TITAN's RFQ ion trap module. The main goal of the TITAN facility is to determine the mass of an isotope with very high precision by employing the Penning Trap mass spectrometry. The RFQ cooler is used to prepare ions, obtained from the TRIUMF's Isotope Separation and Acceleration (ISAC) facility, before the actual mass measurement. The requirements of the RFQ device are 3 MHz coupling frequency and 800 Vpp amplitude. This report presents and explains experimental details, measurement data, and electronic circuit designs.

I would like to thank many people who have helped me during my work term at TRIUMF. In particular, my very special thank is due to Dr. Michael J. Barnes from the Kicker group for being my mentor during the development of this project. I am also grateful to Dr. Joseph Vaz, Matthew Smith, and Dr. H. Sharma for their supports, teaching, and helpful comments and suggestions. I would also like to thank Mr. Mel Good, Mr. Hart Sprenger, Robert Cussons, and Brent van Kleeck for their helps. Most importantly, I would like to thank Dr. Jens Dilling, the project leader and my supervisor, for his supports and the opportunity to work with the TITAN group.

SUMMARY

This report presents the development of a high-voltage RF-DC coupling board for TRIUMF's Ion Trap facility for Atomic and Nuclear science (TITAN) RFQ ion trap beam cooler module. The ion trap module requires a two-dimensional high-frequency magnetic field to confine selected ions of isotopes for mass measurement.

A single-polarity RF prototype driver has been tested up to 3 MHz and 700 Vpp using a pair of RF power MOSFET connected in series. Each power MOSFET, its driver components, and a ferrite pulse transformer are installed on a FET switching board. The pulse transformer allows isolated-operation from the 60 kV high-voltage platform used in TITAN's testing area. Experiments indicated that 301 kHz current pulse and 60V 1.34 A DC supply are necessary to operate the FET switching board at 3 MHz. Modifications to the previous design of the FET board has also been made to allow high-frequency operation. Using a fibre-optic link, the high-voltage pulsing is controlled by electronic circuits that outputs two alternating TTL pulses. To avoid cross-conduction during operation, the pulses are designed to have ~50 ns time gap.

The RF-DC coupling operation requires careful analysis to minimize ringing of the high-voltage pulse observed on the RFQ elements. Minimizing the loop area of the external circuit helps reducing the ringing problem. Also, in order to improve the output pulse, BNC wire is chosen to connect the switching circuit and the RFQ elements.

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LIST OF ABBREVIATIONS

Ω	Ohm
µs	micro second
A	Ampere
AWG	American Wire Gauge
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DEI	Directed Energy Inc.
EBIT	Electron Ion Beam Trap
EMS	Electronic Measurement Inc.
FET	Field-Effect Transistor
HV	High-Voltage
ISAC	Isotope Separation and Acceleration
keV	kilo electron Volt
kHz	kilo Hertz
kV	kilo Volt
LED	Light Emitting Diode
mA	milli Ampere
MBd	Mega Baud
MHz	Mega Hertz
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
mV	milli Volt

nC ..... nano Coulomb

ns ..... nano second

pF ..... pico Farad

PSI ..... Paul Scherrer Institut

RF ..... Radio Frequency

RFQ ..... Radio Frequency Quadrupole

TITAN ..... TRIUMF's Ion Trap Facility for Atomic and Nuclear Science

TRIUMF ..... TRI University Meson Facility

TTL ..... Transistor-Transistor Logic

V ..... Volt

Vpp ..... Volt peak-to-peak

W ..... Watt

1.0 INTRODUCTION

This report presents the development of the radio frequency (RF) high-voltage (HV) driver for TRIUMF's Ion Trap facility for Atomic and Nuclear science (TITAN) Radio Frequency Quadrupole (RFQ) beam cooler module. The RF high-voltage pulsing mode, up to 800 Vpp and 3 MHz, is required by the RFQ module (see Fig. 1) to confine ions in two dimensions for the TITAN experiment at TRIUMF. Currently, a single-polarity HV pulsing for the module has been successfully tested.

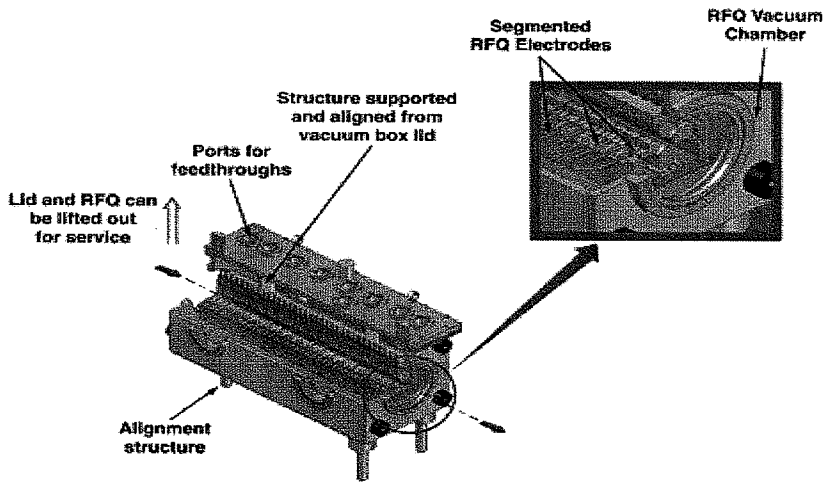

Figure 1. TITAN RFQ Cooler and Buncher [12]

The TITAN project aims for high-precision mass measurement for short-lived radioactive isotopes using the Penning Trap mass spectrometry. The TITAN system consists of the RFQ Cooler, the Electron Ion Beam Trap (EBIT), a Four-Way Switch, the Wien Filter, and the Penning Trap [1]. Prior to the actual mass measurement, the ions have to be specifically prepared in the RFQ cooler and buncher; it is used to decelerate and bunch a 60 keV ion beam taken from the TRIUMF's Isotope Separation and Acceleration (ISAC) facility.

The RFQ forces the ion to move along the z-axis during cooling process with an inert buffer gas without hitting the potential-providing rods and being lost by applying an electric field in two dimensions plane (x- and y-axes). Inside the RFQ, an ion beam can be cooled via collisions with an inert buffer gas. To prevent the beam from diverging, a quadrupole field, which consists of four electrodes (see Fig. 2), is applied; therefore, the electric field traps the ion beam in the x- and y-axes and the field pushes the focused ions onto its z-axis.

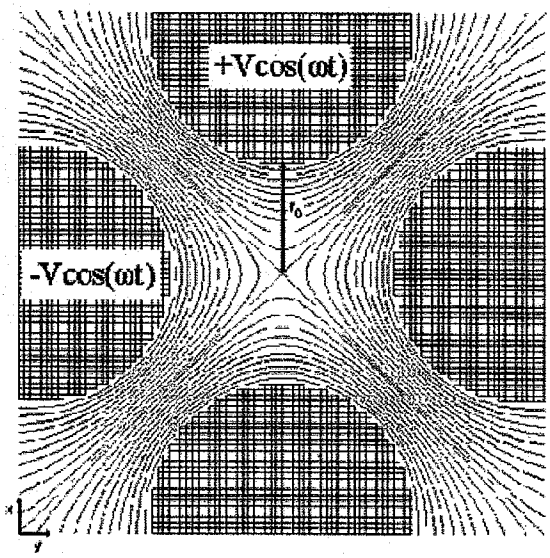

Figure 2. RFQ 2-D Quadrupole Field [13]

The RFQ frequency range affects the variety of isotope species that the TITAN facility can observe. The following formula defines the q-value, which governs the stability of the ion paths in the RFQ:

$$q = \frac{2\,e\,Vpp}{m\,r_o^{2}\,\Omega^{2}}$$

e = ion charge
Vpp = RFQ peak-to-peak voltage
m = ion mass
r_o = RFQ radius
Ω = RF-field angular frequency

The motion of an ion inside an RFQ device is stable for q = 0.908 [2]. Therefore, to keep the stability of ions with very light masses, the RF angular frequency must be increased.

The report is divided into three sections: switching control module, Field-Effect Transistor (FET) switching board module, and single-polarity high-voltage switching operation.

2.0 SWITCHING CONTROL MODULE

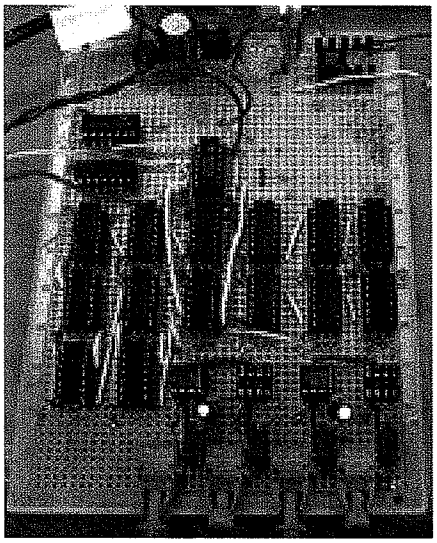

Figure 3. Switching Control Circuit

The switching control circuit, shown in Figure 3, was developed in order to control the timing of the HV pulsing for TITAN's RFQ beam cooler module. The three following sections discuss the timing requirement, the trigger circuit, and the fibre-optic transmitter.

2.1 Timing Requirement

The TITAN's RFQ Module requires a HV pulsing mode with up to 3 MHz switching frequency. This goal can be achieved by connecting two RF power Metal Oxide Semiconductor Field Effect Transistors (MOSFET) in series (see Fig. 4a) and turning each of them on alternatively. The alternating pulses that control the MOSFETs must be identical in terms of their duty cycle. In addition, to prevent cross-conduction during switching operation, both pulses must have an approximately 50 ns time-gap, constant and frequency-independent, between them; this specific time gap was based on experiments. Figure 4b describes the timing diagram of the trigger pulses and the expected 50% duty cycle HV switching output.

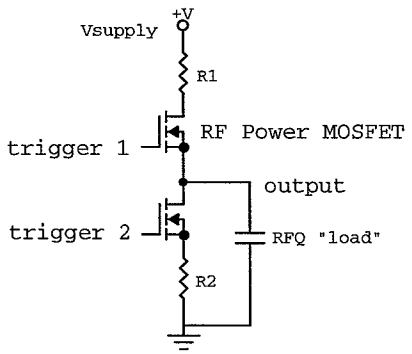

Figure 4a. Basic Switching Circuit using MOSFET

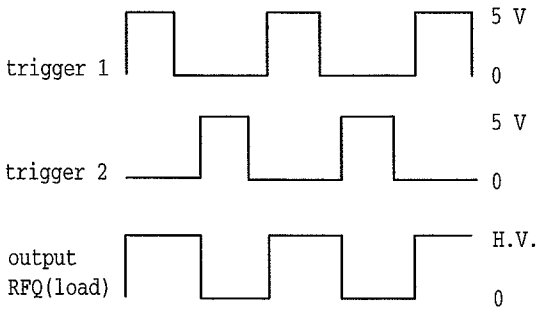

Figure 4b. Trigger Pulses and HV Switching Output

2.2 Trigger Circuit

The trigger circuit design, shown in Figure 5, was selected to produce the two alternating pulses with 50 ns time-gap as described in section 2.1. The circuit consists of "F" (fast) Complementary Metal Oxide Semiconductor (CMOS) chips with 3.7 ns rise-time, essential to enable operation up to 4 MHz.

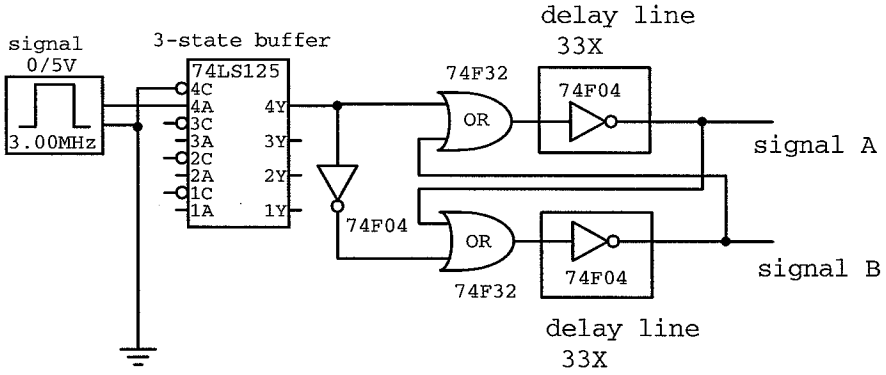

Figure 5. Trigger Circuit Diagram

A square-wave generator, set at 50% duty cycle and 5 volts amplitude, functions as the clock of the circuit. The design features two crossing-feedback inputs to each of the 74F32 OR gates; therefore, the two alternating output pulses (signal A and B) have the same duty cycle. The time gap is determined at 1 V, the low logic threshold for most Transistor-Transistor Logic (TTL) devices. Circuit diagrams of 5

and 15 V power supplies are described in Appendix A. An alternative trigger circuit design is discussed in Appendix B. Figure 6 below shows an oscilloscope snapshot of the trigger signals at 3 MHz switching rate; x-axis (time) represents 100 ns/div and y-axis (voltage) represents 2 V/div. The signals have 5 V-amplitude and the vertical cursors shows 52 ns time-gap.

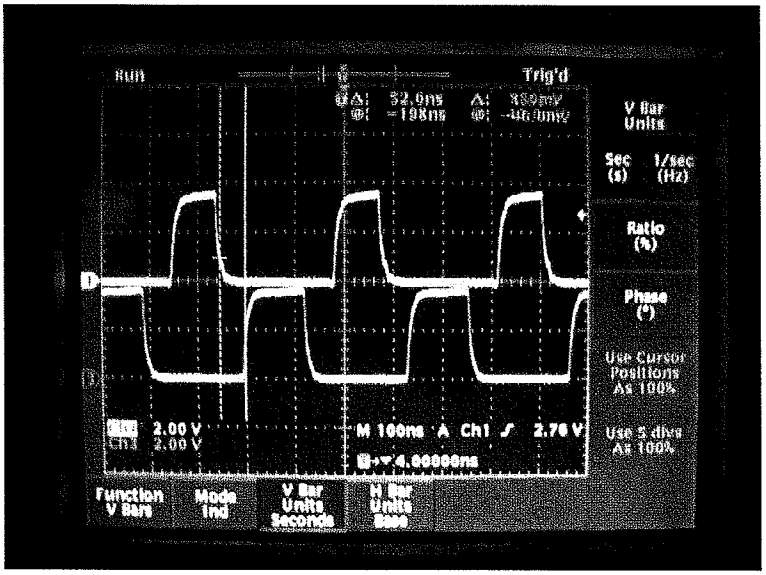

Figure 6. Trigger Signals at 3 MHz Switching Rate

2.3 Fibre-Optic Transmitter

The selection of fibre-optic as the method to provide trigger signals for each FET board is due to two factors:

- The RFQ cooler and buncher module will be installed on a high-voltage (60 kV) platform; thus, the electronics for RFQ must be electrically isolated from the environment.
- The existing FET board (1 kV module) developed by the Kicker group at TRIUMF uses a fibre-optic link to control the RF MOSFET driver and the RF power MOSFET [3].

The HFBR-1528 fibre-optic transmitter was selected because of its compatibility with the HFBR-2528 fibre-optic receiver installed on each of the FET board. This fibre-optic link, called HFBR-0508 series, has an operating range from direct current (DC) to 10 MBd [4]. Each transmitter uses a 650 nm Light Emitting Diode (LED) and requires 60 mA current to operate in the forward-voltage mode. A 74F5300 fibre optic LED driver, from Philips Semiconductor, is required to drive each transmitter (see Fig. 7) because the driver has high driving-current capability (160 mA) and only needs 8 mA input from typical CMOS chips. The LED driver also features an internal TTL input buffer and fast rise-time of 2ns [5].

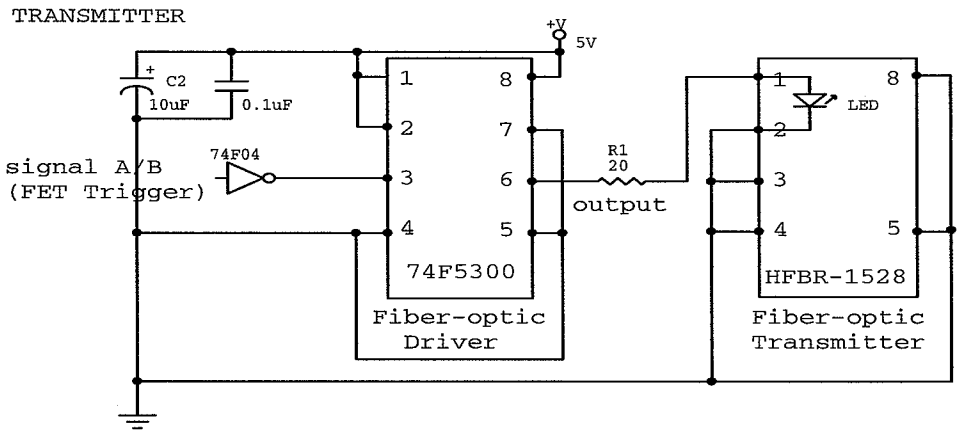

Figure 7. Fibre-optic Transmitter Circuit Diagram

An observation showed that the transmitted signal is inverted at the output of the HFBR-2528 receiver. Thus, to have correct signals controlling the MOSFET drivers on FET boards, the trigger signals must be inverted at the transmitter's side using a 74F04 Hex Inverter (see Fig. 7). Figure 8 shows an oscilloscope snapshot of the transmitted signals at 3 MHz switching rate; x-axis (time) represents 100 ns/div and

y-axis (voltage) represents 2 V/div. The signals have 5 V-amplitude and the vertical cursors shows 52 ns time-gap.

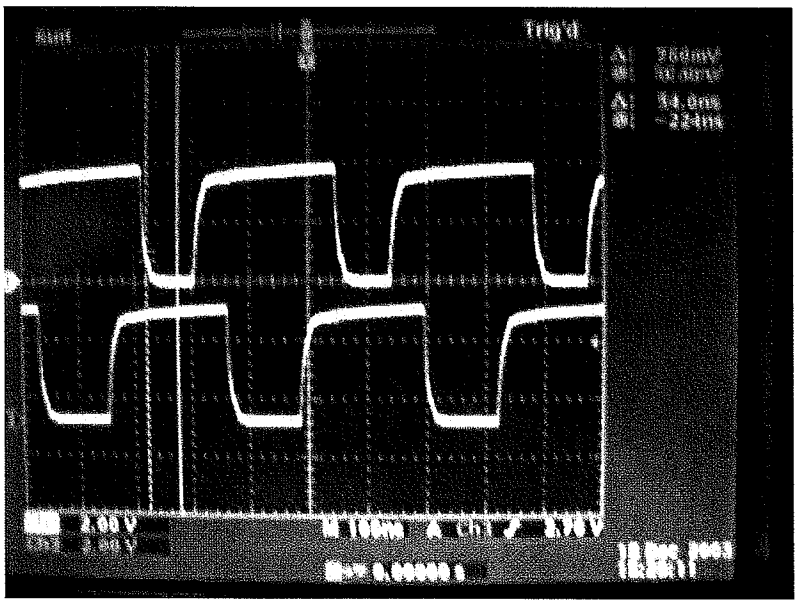

Figure 8. Transmitted Signals at 3 MHz Switching Rate

3.0 FET SWITCHING BOARD MODULE

The FET switching board, shown in Figure 9, was initially developed by the Kicker group at TRIUMF for the "MuLan" experiment at the Paul Scherrer Institut (PSI) in Switzerland [1]. The three following sections discuss the power supply, the main components of the FET board, and modifications made for the RFQ ion trap.

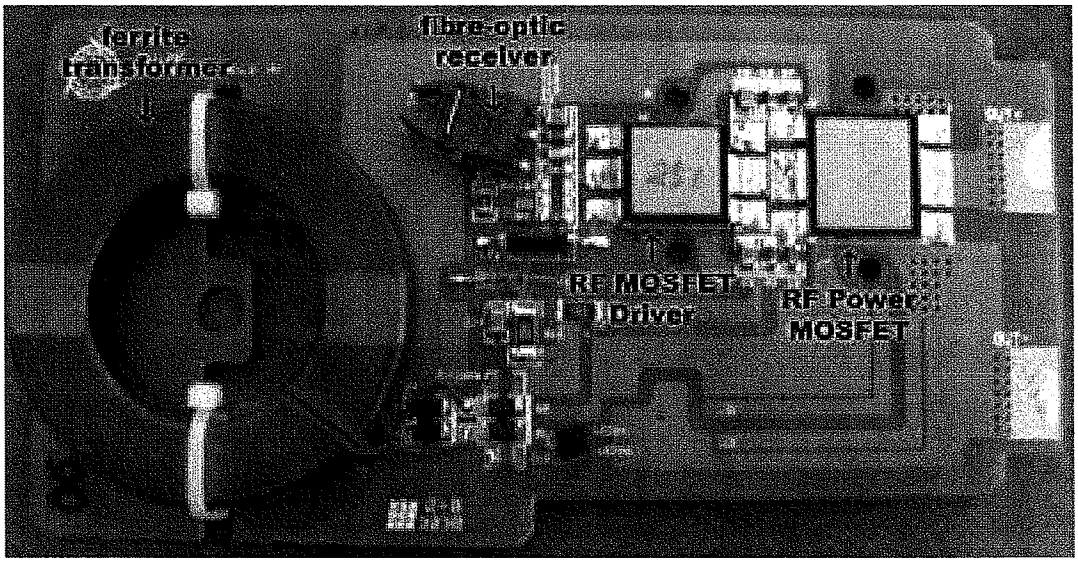

Figure 9. FET Switching Board

3.1 Power Supply

Each FET switching board has a ferrite pulse transformer and requires a current pulse on its primary side. Therefore, to provide DC voltage to each FET board, one must create a current pulse with specific amplitude and rate, corresponding to the RFQ switching rate. This power supply section incorporates the use of a high-current DC power supply and a current pulse generator board (see Fig. 10), also previously developed by the Kicker group at TRIUMF. The following two sections discuss the ferrite pulse transformer and the current pulse.

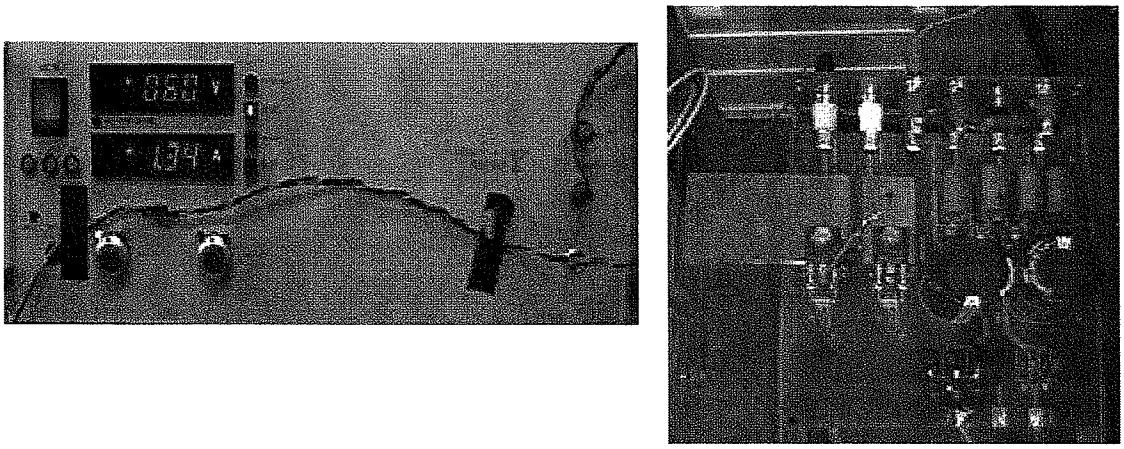

Figure 10. High-Current DC Power Supply and Current Pulse Generator Board

3.1.1 Ferrite Pulse Transformer

During HV switching, each FET board must be electrically isolated from the switching ground. Therefore, to operate its electronic components, each FET board utilizes a ferrite pulse transformer with two turns on its secondary (see Fig. 11a). Several FET boards can use a single primary wire that carries a current pulse (see Fig. 11b). Then, the transformer and a full-wave rectifier circuit regulate a DC voltage on each FET board. Details regarding the current pulse regulation into DC voltage are discussed in Appendix C.

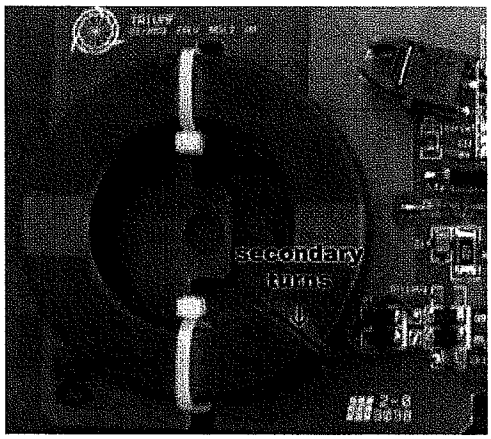

Figure 11a. Ferrite Pulse Transformer

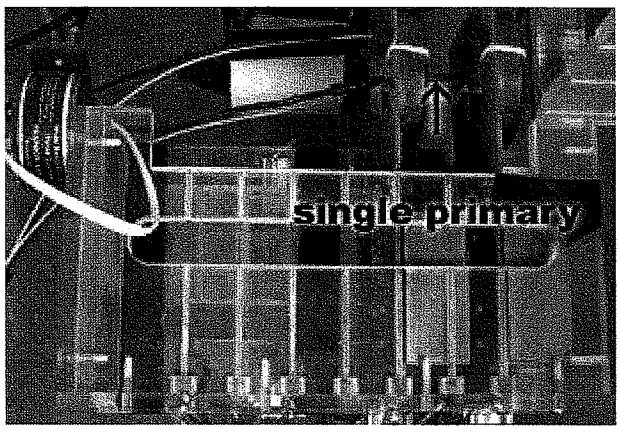

Figure 11b. Single Primary Wire

3.1.2 Current Pulse

The magnitude of the DC voltage, produced by the ferrite transformer's secondary and indicated by a yellow LED, depends on the DC supply voltage and the rate of the current pulse. Figure 12a shows an oscilloscope snapshot of the current pulse, carried by the primary wire, at 301 kHz and 264 mVpp; x-axis (time) represents 1 μs/ div and y-axis (voltage) represents 100 mV/div. To operate the FET board properly, one should measure a 16 V potential across the C13 capacitor on each FET board. However, the measurement cannot be conducted during HV pulsing because the measurement probe will cause interference to the electronics. The RFQ switching rate determines the DC voltage and current required, as well as the current pulse rate. Experiments indicated that a 60 V DC supply (~1.34 A) and a current pulse rate of 301 kHz are necessary to operate a pair of FET boards at 3 MHz RFQ switching frequency. Measured data, graphs, and details describing the relation between the current pulse rate and the RFQ rate (without HV pulsing) are discussed in Appendix D.

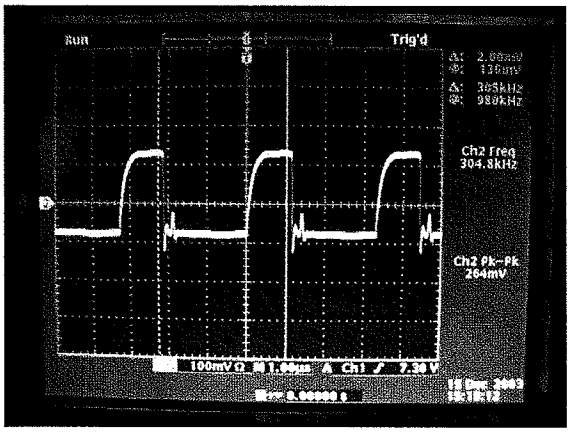

Figure 12a. Current Pulse

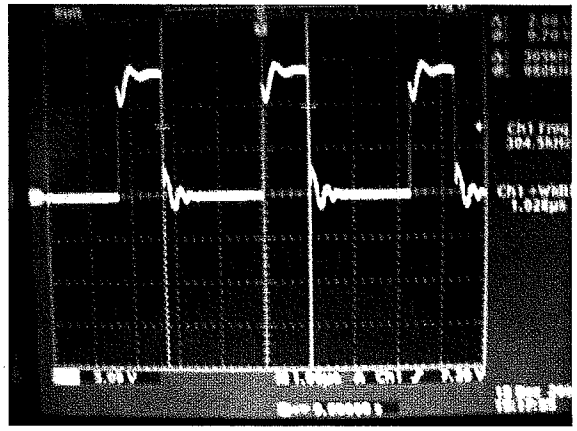
Figure 12b. Amplified 1 μs TTL Pulse

The current pulse rate is controlled by a TTL (0/5 V) pulse, generated by a square-wave generator, set on a constant 1 μs pulse width. The TTL pulse controls the APT1001RBN Power MOSFET [6] through the MIC4420 MOSFET Driver [7]. The MOSFET driver amplifies the TTL pulse to 0/15 V pulse (see Fig. 12b) and controls the APT Power MOSFET, on the current pulse generator board, through a coaxial cable. Figure 12b shows an oscilloscope snapshot of the amplified 1 μs TTL pulse, at 301 kHz and 15 Vpp; x-axis (time) represents 1 μs/ div and y-axis (voltage) represents 1 V/div. Increasing the current pulse rate increases the DC voltage on FET board and causes more current to be drawn from the DC supply; however, experiments showed that increasing the current pulse rate above 400 kHz is not effective for providing 16 V (DC) on FET board; therefore, the amplitude of the current pulse needs to be increased by increasing the DC supply voltage.

The high-current DC supply connected to the current pulse generator board determines the amplitude of the current pulse carried by the primary wire. Experiments show that a 60 V DC supply and 341 kHz current pulse rate enable operation of two FET boards up to 3.5 MHz. Figure 13 describes the overall circuit diagram for the FET power supply. Prior to feeding current pulse to each ferrite transformer, current from the 60 V DC supply passes a smoothing circuit and a power resistor (~8 Ω). The power resistor is required to limit the maximum current during pulsing. The magnitude of the current

pulse (~2.6 A) can be monitored by using a current transformer that indicates 100 mV per 1 A as shown in Figure 12a.

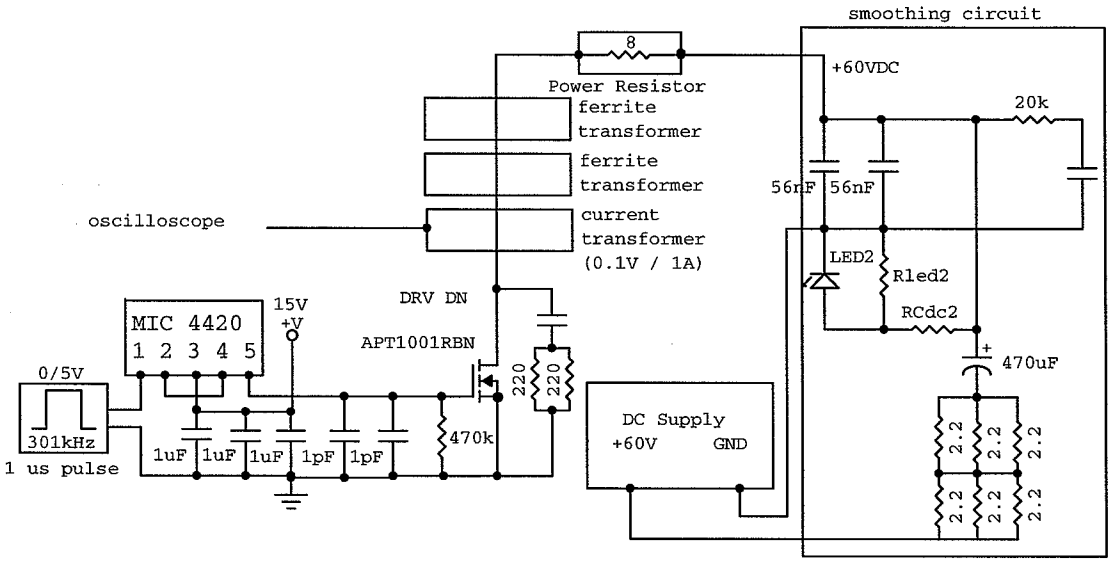

Figure 13. Current Pulse Circuit Diagram

3.2 Main Components of the FET Board

The HV pulsing required for TITAN's RFQ module uses the existing FET Board developed by the Kicker group at TRIUMF [3]. The circuit diagram of the FET board is shown in Appendix E. The three following sections discuss the main components of the FET board, which consists of a fibre-optic receiver, a RF MOSFET Driver, and a RF Power MOSFET.

3.2.1 Fibre-Optic Receiver

The HFBR-2528 fibre-optic receiver was chosen to provide the CMOS/TTL trigger signals and to directly control the RF MOSFET driver. The fibre-optic link operates from DC to 10 MBd. The DC rating is important as it minimizes the susceptibility too erratic switching due to noise [3]. As mentioned in

section 2.3, the output signal from the receiver inverts the actual light pulses transmitted by the HFBR-1528 fibre-optic transmitter.

The fibre-optic receiver is covered with a copper shield, which protects the unit from noise due to electric field; the shield also functions as a heatsink. The maximum operating temperature of the receiver is 85°C [4]; however, keeping the temperature below 60 °C is recommended.

3.2.2 RF MOSFET Driver

The DEIC420 RF MOSFET Driver is a CMOS high-current gate driver with wide operating range (8-30 V) and a fast rise/fall-time of 4 ns [8]. The selection of DEIC420 was also based on its ability to sink/source high currents (20 A), minimum pulse width (8 ns), and package compatibility with the DE375-102N12A RF power MOSFET [3].

This MOSFET driver has the same maximum operating temperature (85°C) as the fibre-optic receiver [8]; therefore, both devices are covered by a single copper-shield.

3.2.3 RF Power MOSFET

The DE375-102N12A RF Power MOSFET, from Directed Energy Inc. (DEI), is a N-Channel Enhancement Mode FET with 1 kV voltage rating, 50 MHz maximum frequency, and high dv/dt [9]. The selection of this power

MOSFET was based upon high peak repetitive pulse current (72 A), low gate charge (93 nC), fast turn on (3 ns) and turn-off (8 ns). To switch the DEI FET rapidly, a peak gate current of 12 A is required [3]; hence, the DEIC420 driver was selected as the MOSFET driver.

The maximum junction temperature of the DE375 MOSFET is 175°C [9]. A copper heatsink with large surface area and forced air-cooling are essential to dissipate heat, the result of high power dissipation.

3.3 Modifications for RFQ Ion Trap

A series of two FET boards were already tested by the Kicker group to operate at 800 V and 500 kHz [3]. For TITAN's RFQ Cooler and Buncher module, running up to 3 MHz, the same circuit configuration shown in Appendix E was used; only two simple modifications, changing the value of R10 and increasing the surface area of the FET heatsink, were made to increase the high-frequency switching capability.

3.3.1 Value of R10

The previous configuration of the1 kV module utilized a 4.7 Ω 0.25 W surface-mounted resistor, called R10 (see Fig. 14), for these reasons [10]:

a) To measure the current drawn by the FET driver by measuring the voltage drop across R10

b) To limit the current drawn by the FET driver; initially, there was a problem with the 16V voltage on the FET card coming up properly during

start-up. R10 was used to check whether the problem was due to the FET driver.

c) To define where the transient current flows when the FET driver turns on and off the FET; R10 limits the transient current drawn from C13.

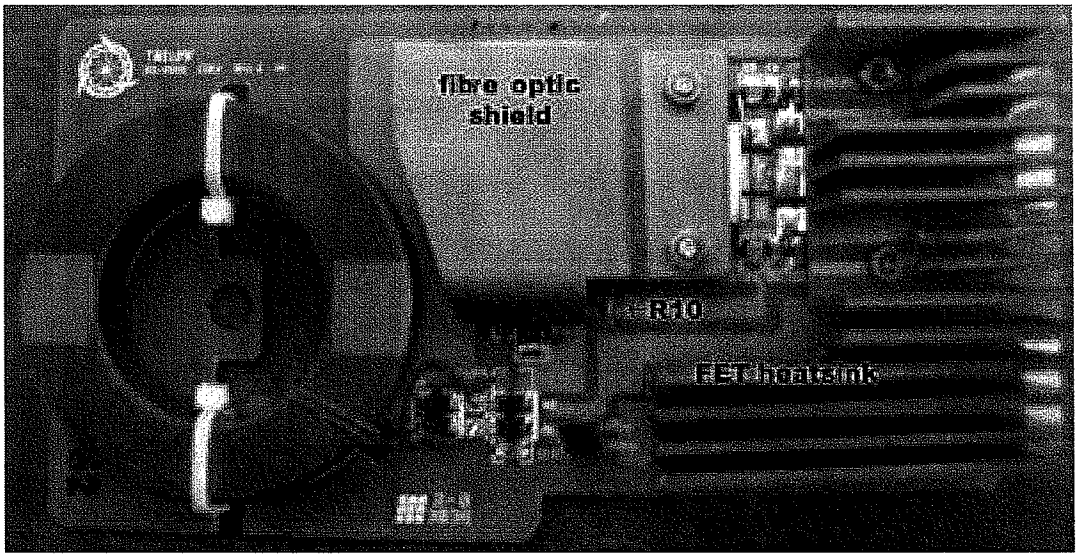

Figure 14. Modified FET Switching Board

According to Dr. Barnes, from the Kicker group at TRIUMF, operating each FET board at 3 MHz would likely to draw approximately 0.6 A through the 4.7 Ω resistor and exceed its power rating (1.6 W) [11]. Therefore, it was suggested that a 1.2 Ω 1 W surface-mounted resistor is needed to replace the existing 4.7 Ω resistor (R10).

3.3.2 FET Heatsink

The original FET heatsink used for the "MuLan" experiment is a single cooper sheet with approximately 26-cm2 surface area. During experiment for TITAN's RFQ module, the temperature of the original heatsink reached 90°C at 2 MHz and 700 Vpp pulsing. High operating temperature reduces the

performance of the MOSFET and causes power supply instability in long duration. Hence, the heatsink was replaced with one that has fins (see Fig. 14); the surface area is increased to approximately 210 cm^2. As the result, the operating temperature of each MOSFET at 3 MHz and 700 Vpp is ~50 °C.

4.0 SINGLE-POLARITY HIGH-VOLTAGE SWITCHING OPERATION

Prior to operating the RFQ ion trap with two polarities, a single-polarity HV switching operation, on the vertical axis of the RFQ ion trap, has been tested up to 3 MHz and 700 Vpp; the horizontal axis of the RFQ ion trap is connected to the ground of the switching power supply. The switching power supply used during experiment is a positive DC power supply, from Electronic Measurements Inc. (EMS), rated for 600 V maximum. The three following sections discuss the circuit connection, the RFQ capacitive load, and the RFQ switching output for single-polarity HV pulsing.

4.1 Circuit Connection

The circuit connection for single-polarity HV switching operation, shown in Figure 15, requires a careful analysis to minimize the circuit inductance that greatly affects the HV pulsing output. The inductance in the circuit, proportional to the loop area, causes ringing on the HV pulsing output; therefore, the loop area needs to be minimized by shortening and twisting wire connecting the HV switching circuit to the capacitors and power supply.

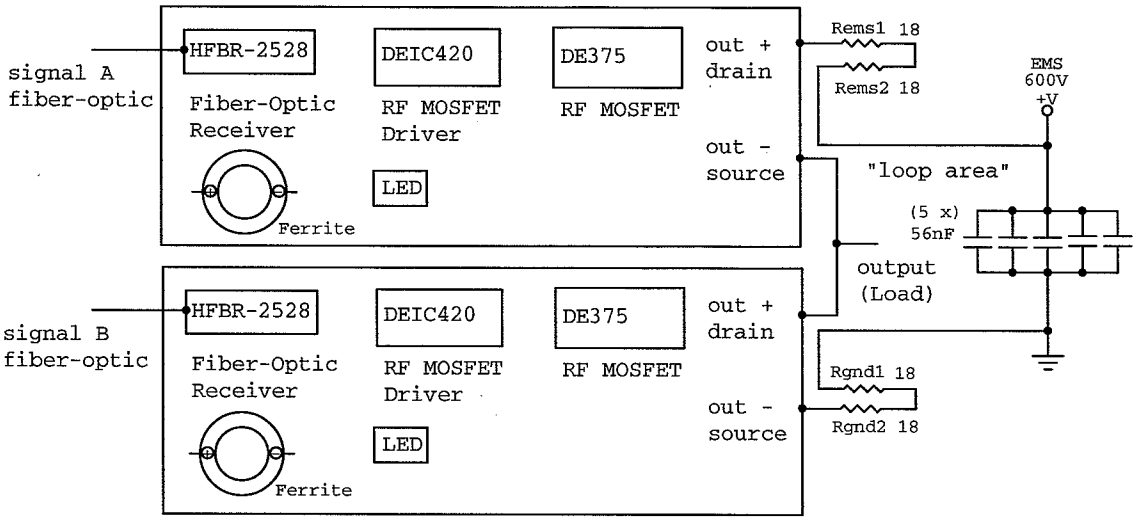

Figure 15. HV Switching Circuit

The power resistors, on each side of the power MOSFET, limit the amount of current drawn through the MOSFET from the power supply. The resistance value on each side must be equal to balance dv/dt (rise-time and fall-time) of each MOSFET during pulsing.

The type of wire connecting the MOSFET circuit output to the RFQ device needs a careful consideration. 14 AWG 1 kV-rated wire provides fast conduction (minimum capacitance) from the MOSFET circuit to the RFQ device, but the wire may cause problem with inductance as its length and loop area increases. Meanwhile, coaxial cable reduces the inductance problem, although the cable introduces additional load capacitance that slightly slows down the conduction. For single-polarity HV testing purpose, the RFQ elements in each axis are connected together using 14 AWG wire and a coaxial cable is used to connect the MOSFET circuit to the RFQ device (i.e. the single conductor of coaxial cable connects the output of the MOSFET circuit

and the vertical RFQ elements, and the outer conductors connect the horizontal RFQ elements and the ground of the switching power supply).

4.2 RFQ Capacitive Load

Based on a measurement, the complete set of RFQ elements (24 segments), shown in Figure 16, has a capacitive load of 104.8 pF. For double-polarities HV switching, the capacitive load is likely to increase by a factor of 2 due to a virtual ground between the polarities during pulsing; the amount of current drawn from the switching power supply is likely to increase as well. Appendix H provides a recommendation for double polarities HV switching operation. Detail drawings of RFQ assembly are shown in Appendix I.

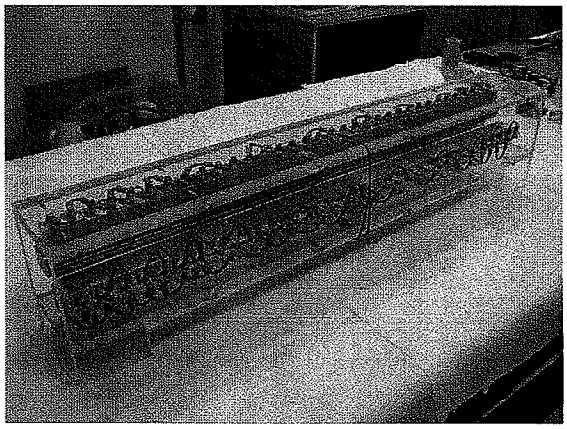

Figure 16. RFQ Set-Up

4.3 RFQ Switching Output

Figure 17 shows the waveform of the RFQ switching output at 3 MHz. The maximum amplitude of the HV pulse has been tested and measured up to 700 Vpp due to the measurement probe limitation (rated for 670 V max). This HV pulse amplitude, however, is not indicated by the EMS power supply reading, which

shows 500 V and 0.81 A. Figure 17 shows an oscilloscope snapshot of the 3 MHz switching rate; x-axis (time) represents 100 ns/div and y-axis (voltage) represents 100 V/div. According to the oscilloscope measurement, the 3 MHz HV pulse has 700 Vpp-amplitude, 18.5 ns rise-time, 22 ns fall-time, and 55% duty cycle. The procedure for single-polarity HV switching operation is discussed in Appendix F.

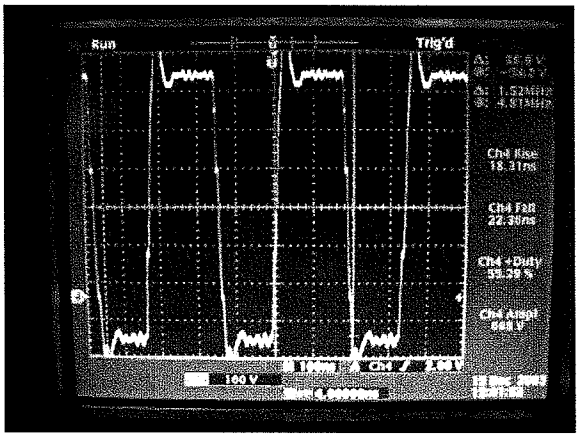

Figure 17. HV Pulse at 700 Vpp and 3 MHz

During HV switching operation, the amount of current drawn from the DC power supply (for the current pulse), discussed in section 2.1.2, increases by 0.01 – 0.04 A from the initial FET board power supply measurement (see App. D). This condition is normal as long as the amount of current, indicated by the DC power supply does not fluctuate. Other measured data, including temperature reading, of single-polarity HV pulsing are described in Appendix G.

An observation using an oscilloscope shows that connecting the output of the HV switching circuit to the middle of the RFQ axis reduces the rise-time difference of the HV pulse on RFQ elements. The current will travel from the middle of the axis to its edge and come back to the middle; therefore, the HV pulse at the middle of the axis has a slightly longer rise-time due to the "reflection". The final RF drive

electrical configuration for TITAN's RFQ cooler, however, will have a direct connection from the HV switching circuit output to each pair-segment RFQ elements, as shown in Appendix J.

5.0 CONCLUSION

The HV pulsing for TITAN's RFQ cooler and buncher has been successfully tested up to 3 MHz and 700 Vpp for single-polarity operation. It is, however, possible to increase the pulsing rate up to 3.5 MHz with current electronic configuration of the FET switching boards. The high-voltage amplitude was not tested beyond 700 Vpp because of the measurement probe limitation. Single-polarity HV switching at 3 MHz and 700 Vpp requires a 500 V and ~0.81 A from a DC power supply.

The FET switching boards, electrically isolated from the 60 kV platform, required a current pulse to operate. The current pulse is controlled by the current pulse generator board that requires a DC power supply. The amount of current drawn from the power supply is dependent on the RFQ frequency. Based on experiments, HV pulsing with 2 FET boards, operating at 3 MHz and 700 Vpp, requires 60V DC and ~1.34 A.

The HV pulsing operation for RFQ requires a careful analysis of the circuit connection, the RFQ capacitive load in order to reduce ringing on the HV pulse, the switching output. The ringing is usually due to the inductance in the HV switching circuit, proportional to the loop area; hence, the area needs to be minimized as much as possible. To improve the HV output pulse, a BNC wire, which has low inductance, is used to connect the HV switching circuit and the RFQ elements. Connection to the middle of the RFQ axis is essential to minimize the rise-time difference of the RFQ elements.

6.0 RECOMMENDATION

The following recommendations present main steps for single-polarity HV pulsing operation for TITAN's RFQ beam cooler and suggestions for developing HV pulsing system with two polarities.

To operate single-polarity HV pulsing for TITAN's RFQ using a series of two FET switching boards, one needs to follow the following procedure:

1. Ensure that the switching control outputs two alternating signals with at least 50 ns time-gap and the signals must be inverted prior to transmission via fibre-optic
2. Ensure that the current pulse rate matches the requirement, determined by the RF-field rate as shown in Appendix D
3. Ensure that the cooling fans are turned on prior to HV switching operation

Further details regarding the single-polarity HV switching operation procedure are discussed in Appendix F.

To continue operating HV pulsing for TITAN's RFQ with two polarities, there are some factors that need to be carefully observed:

1. The trigger signals controlling the HV switching operation needs to have sufficient time-gap to prevent cross conduction; the development of switching control module using FPGA or microcontroller, for easy adjustments, is recommended

2. The current pulse rate and amplitude, corresponding to the DC voltage supply, required to apply 16 V on each FET board (measured across the C13 capacitor)
3. The stability of the DC power supply for the current pulse prior and during HV pulsing operation
4. The power consumption and temperature reading of the RF power MOSFETs and the power resistors during HV pulsing operation
5. The inductance of the HV switching circuit that may cause ringing on the HV output pulse

Further details of recommendation for double-polarities high-voltage switching are discussed in Appendix H.

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APPENDIX A

Positive 5 and 15 V Power Supply Circuit Diagram

The circuit diagram below is the positive 5 and 15 V power supplies used to power up the trigger circuit and the MIC4420 MOSFET driver, shown in Figure 1. The trigger circuit consists of CMOS chips that need 5 V power supply and the MOSFET driver requires 15 V power supply to amplify the 1 μs TTL pulse to control the current pulse.

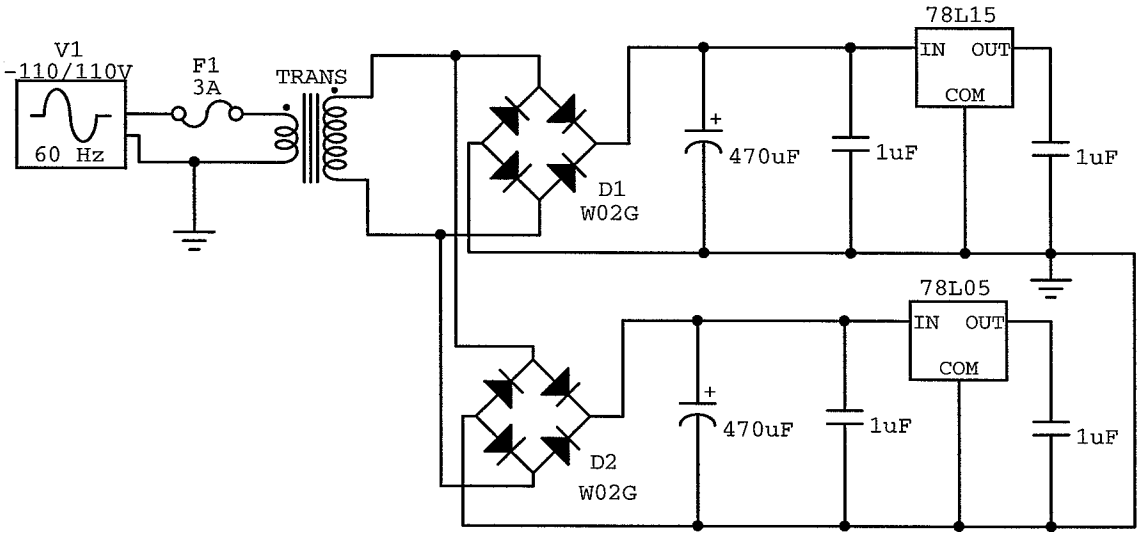


Figure A1. Positive 5 and 15 V Power Supply

APPENDIX B

Alternative Trigger Circuit Diagram

The figure below is an alternative trigger circuit used to control FET switching. Similar to the design shown in Figure 5, this alternative trigger circuit requires "F" CMOS chips to enable high-frequency operation. The operating frequency limit was never tested, although the design is able to output two alternating signals up to 3 MHz with 50 ns time-gap. Observations showed that the output signals of the alternative trigger circuit are less square than the output signals of the circuit shown in Figure 5.

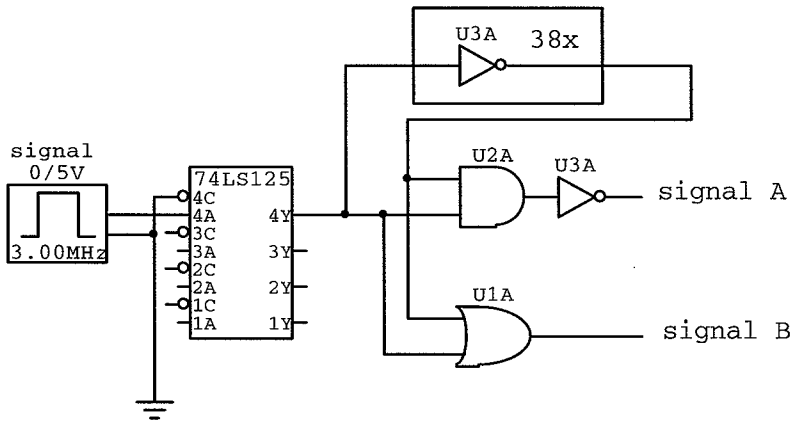


Figure B1. Alternative Trigger Circuit

APPENDIX C

Current Pulse Regulation into DC Voltage

To operate the FET switching board, each board uses a ferrite transformer and a full-wave rectifier circuit. The ferrite transformer has two turns on secondary and a single turn on primary, carrying a current pulse. The full-wave rectifier, consisting of 4 fast-high current diodes (ES1B), and approximately 4 μF surface-mounted capacitors provide the 16 VDC power supply on-board [3]. The rectifier circuit converts the di/dt of the current pulse (rising- and falling-edges) into two current phases to derive the DC voltage.

The current pulse, discussed in section 3.1.2, is controlled by the APT1001RBN MOSFET, which utilizes a high-current DC power supply. High-current pulsing through the MOSFET creates the two current phases, then rectified on each FET board. During the activation of the APT MOSFET (rising-edge), the response-time is $^{L}/_{R,}$ where L is the internal inductance and R is the limiter resistance provided by an external power resistor (~8 Ω). However, during the deactivation of the MOSFET (falling-edge), there is an additional resistance due to the "open circuit", which causes large response-time. The response-time corresponds to the current flowing through the MOSFET; therefore, large response-time causes high power dissipation, as described by the following formula:

$$\frac{1}{2} L I^2 = \frac{1}{2} C V^2$$

Figure 13 shows a series of capacitor and resistor connected across the drain-source of the APT MOSFET. This additional circuit is meant to reduce the internal inductance and the power dissipation of the MOSFET.

The gating of the APT MOSFET is provided by the MIC4420CT MOSFET driver, controlled by a TTL pulse from a square-wave generator. The generator is set to output a TTL pulse with 1 μs constant pulse width. Then, the MOSFET driver amplifies the TTL pulse to 0/15 V to control the APT MOSFET. In experiment, the MIC4420CT output is connected to the gate of the APT MOSFET via a BNC (coaxial) cable. This connection causes a little distortion to the 0/15 V pulse, shown in Figure 12b. The distortion occurs due to the APT MOSFET high-impedance, causing "reflection" back to the MIC4420CT.

HV pulsing operation may cause interference to the current pulse; therefore, monitoring the current pulse using a current transformer is necessary to ensure the stability of the high-current DC power supply. A toroid winding (approximately 14 turns), located near the power supply output, creates a large self-inductance to damp any oscillations that may be fed back the DC power supply from the current pulse generator board.

APPENDIX D

Power Supply Measurement Data for FET Board

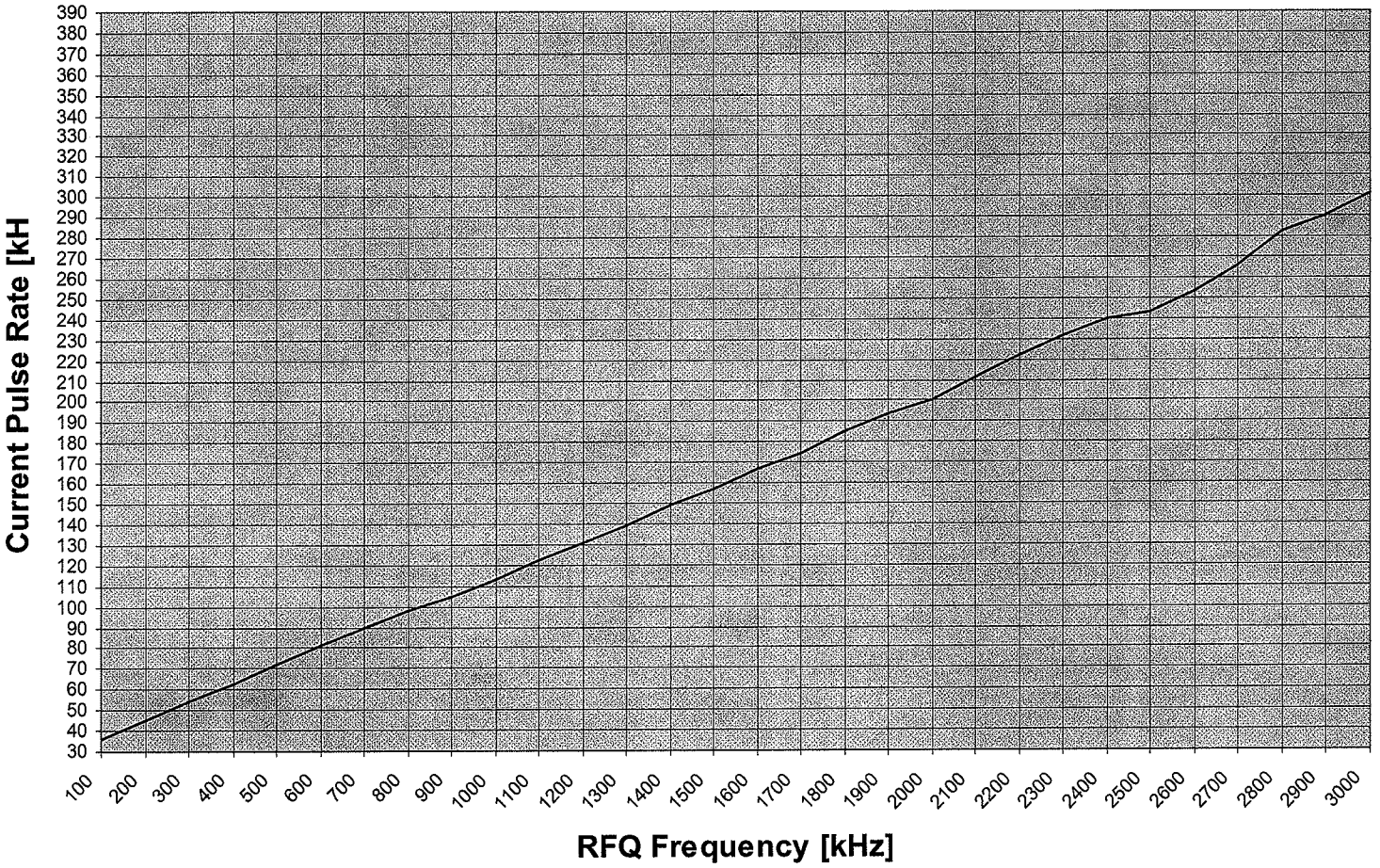
The following illustrations present the power supply measurement data for FET Board and the relationship between the current pulse rate and the RFQ frequency (no HV pulsing). Two FET boards are operated with ~16 V up to 4 MHz using a current pulse, generated by the current pulse generator board; the board uses a DC 60 V power supply. Data show that two FET boards are able to operate normally up to 3.5 MHz.

Table D1. Power Supply Measurement Data for FET Board

RFQ Freq [kHz]	Current Pulse [kHz]	FET #137 top [V]	FET #62 bottom [V]	DC 60V current [A]
100	36	16.10	15.99	0.17
200	45	16.09	16.01	0.21
300	54	16.07	16.03	0.25
400	63	16.07	16.04	0.29
500	72	16.07	16.05	0.33
600	81	16.07	16.05	0.37
700	90	16.07	16.06	0.41
800	98	16.02	15.99	0.44
900	105	16.02	16.04	0.48
1000	113	15.98	15.99	0.52
1100	122	15.97	16.01	0.56
1200	131	16.02	15.98	0.60
1300	139	15.96	16.04	0.63
1400	149	16.00	16.01	0.68
1500	157	16.09	16.00	0.71
1600	167	16.00	16.04	0.75
1700	174	16.00	16.03	0.78
1800	185	16.10	16.01	0.83
1900	194	16.06	16.01	0.87
2000	200	16.12	15.87	0.89
2100	211	16.12	16.01	0.94
2200	222	16.24	15.79	0.98
2300	231	15.97	16.00	1.02
2400	240	15.80	16.48	1.06
2500	243	15.88	16.14	1.07
2600	253	16.30	15.67	1.11
2700	266	16.36	15.56	1.17
2800	283	16.30	15.76	1.24
2900	290	15.89	16.00	1.27
3000	301	15.71	16.64	1.30
3500	*341*	*16.75*	*15.22*	*1.46*
4000	*381*	*14.93*	*16.05*	*1.63*

Figure D1. Current Pulse Rate vs. RFQ Frequency

For 2 FET Boards w/ DC 60V supply



APPENDIX E

1 kV Module Circuit Diagram

The circuit diagram below is the original configuration of the FET switching board (courtesy of Dr. Barnes from the Kicker group).

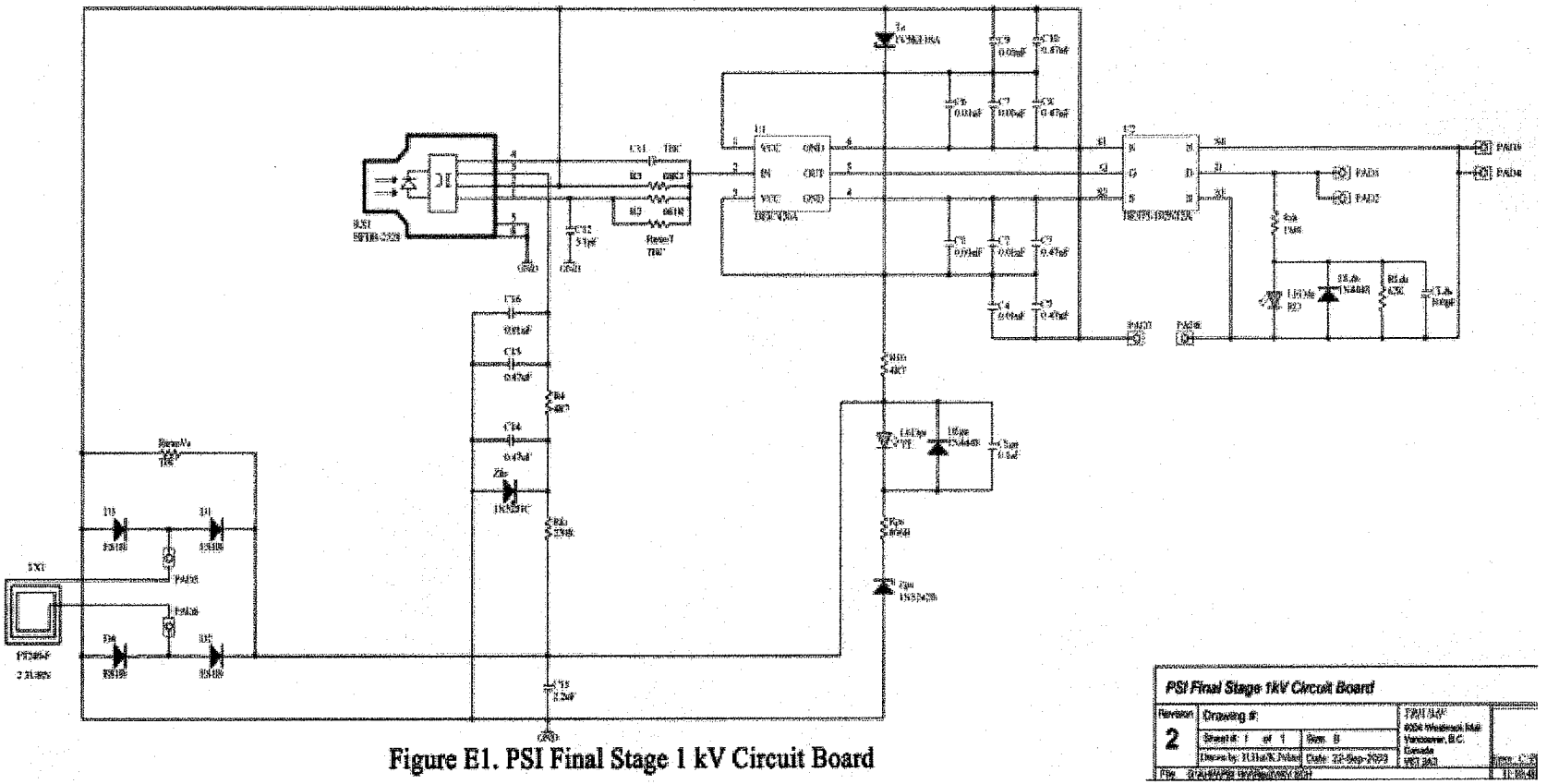


Figure E1. PSI Final Stage 1 kV Circuit Board

APPENDIX F

Single-Polarity High-Voltage Switching Operation Procedure

The following procedures explain the measurement steps and the operation for single-polarity HV switching operation.

F.1 Checking Trigger Signals

1. Adjust the amplitude and offset of the square-wave generator for RFQ drive frequency (see Fig. F1), so that the output pulse is 5 V up to 3 or 4 MHz

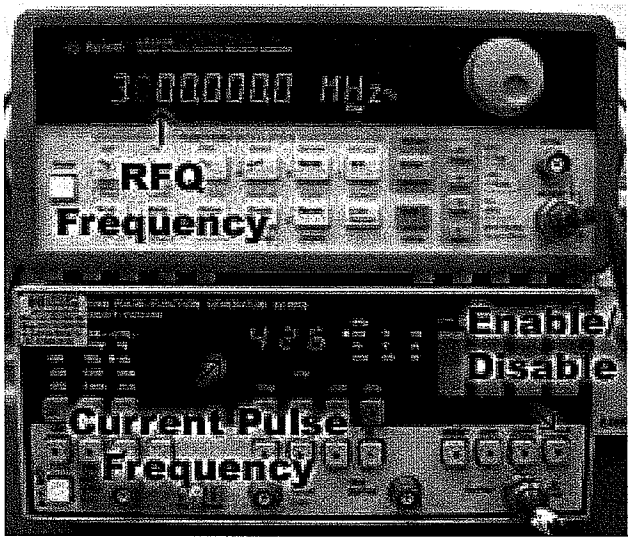


Figure F1. RFQ and Current Pulse Frequency Generators

2. Connect the generator's output to the input of the trigger circuit, the 74125 buffer chip, using a coaxial cable and a T-connector (see Fig. F1); place a 50 ? BNC terminator at the other end of the T-connector.
3. Turn on the 5 V power supply for the trigger circuit
4. Check the output signals of the trigger circuit at the 74F04 hex inverter (pin 5 and 9), as shown in Figure F2a; the signals should look like signals in Figure 6.

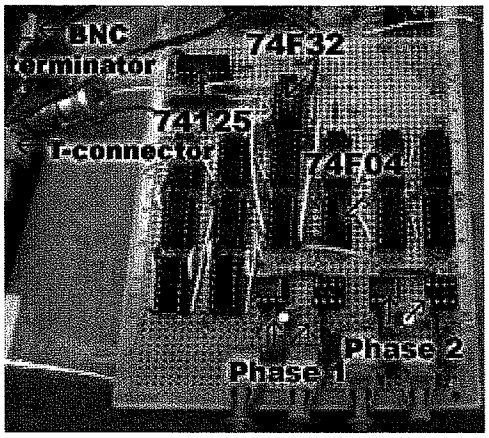


Figure F2a. Trigger Check-points

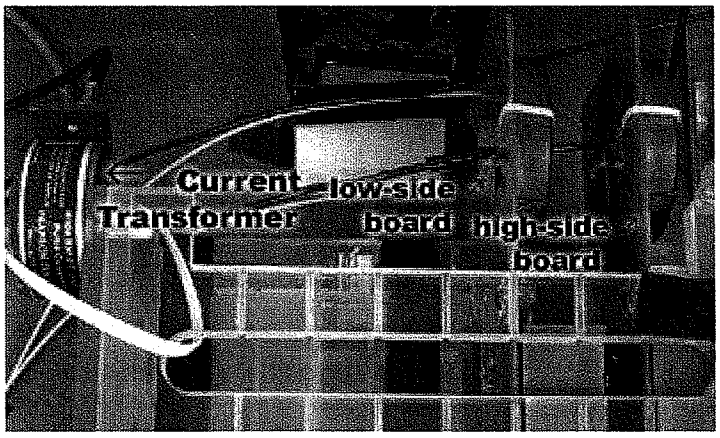


Figure F2b. High-side and Low-side FET Boards

5. Check the transmitted signals at each of 74F5300 fibre-optic driver (pin 3 and 6); the signals should look like signals in Figure 8.
6. Connect one of phase 1 outputs to a low-side FET Board and one of phase 2 outputs to a high-side FET Board (see Fig. F2b) using fibre-optic cables.

F.2 Checking 1 μs Control Pulse for Current Pulse

1. Adjust the amplitude and offset of the square-wave generator for current pulse frequency (see Fig. F1), so that the output pulse is 5V and the pulse width is 1 μs, constant and frequency-independent
2. Connect the generator's output to pin 1 of MIC4420CT
3. Connect the MIC4420CT output (pin 5) to the input of APT1001RBN MOSFET using a T-connector and a coaxial cable; place an oscilloscope probe at the other end of the T-connector
4. Turn on the 15 V power supply for MIC4420CT
5. Enable the square-wave generator's output (see Fig. F1); the 0/15 V output pulse should look like the pulse in Figure 12b.

F.3 Measuring FET Board Power Supply

1. Ensure that the FET boards, the current pulse generator board, the single primary wire, the DC power supply, and the current transformer are connected as shown in the current pulse circuit diagram (see Fig. 13). The arrow sign of the current transformer must be adjacent and opposite to the current direction (toward the smoothing circuit output).
2. Connect the current transformer to an oscilloscope using a coaxial cable. The expected output is 100 mV for every 1 A carried by the primary wire. You need to set 50 ? impedance on the oscilloscope's channel; otherwise, you will need a T-connector and a BNC 50 ? terminator.
3. Proceed with the steps on section F.2 (1 μs Control Pulse for Current Pulse)
4. Turn on the trigger circuit and the cooling fans, and match the current pulse rate and the RF frequency (see Table D1)
5. Turn on the high-current DC power supply (see Fig. 10), press "HV ON" button, ensure that the voltage reading shows 60 V
6. Check the current reading (see Table D1), and ensure that the current reading is stable; otherwise turn off the power supply, and check the current pulse circuit and the 1 μs control pulse again. The current pulse, monitored using the current transformer, should look like the pulse in Figure 12a.
7. Measure the potential across the C13 capacitor on each FET board; the measured potential should be approximately 16 V.

F.4 Adjusting RFQ frequency with DC power supply ON

- Increasing the RFQ frequency: increase the RFQ frequency (3.5 MHz max), then increase the current pulse rate accordingly (see Table D1)
- Decreasing the RFQ frequency: decrease the current pulse rate, then decrease the RFQ frequency accordingly (see Table D1)

F.5 Measuring RFQ Capacitive Load

1. Connect all elements in an axis together using 14 AWG wire (not applied for the final RF drive configuration)
2. At the middle of the axis, connect the vertical pair together; also connect the horizontal pair together (see Fig. F3)

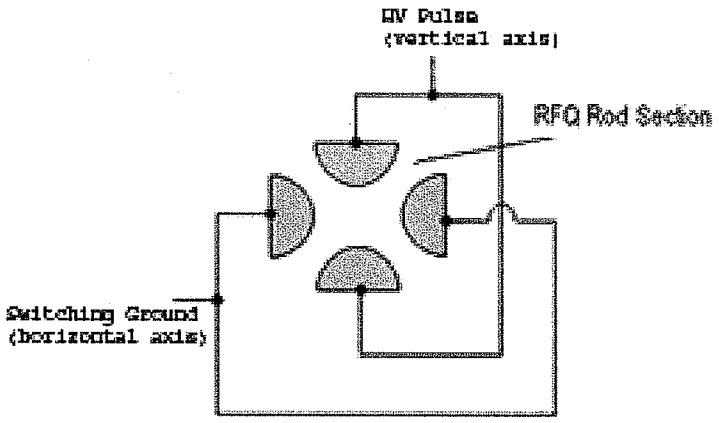


Figure F3. RFQ Pair Connection

3. Measure the RFQ capacitive load using Fluke PM6306 capacitance meter (please consult Dr. Barnes from the Kicker group at TRIUMF)

F.6 Operating Single-Polarity High-Voltage Pulsing

1. Check the HV switching circuit connection as shown in Figure 15

2. Connect the HV switching circuit output and the pair-connection (step 2 of section F.5) using a coaxial cable; the single conductor connects the circuit output and the RFQ vertical pairs, while the outer conductors connect the ground of the switching power supply and the RFQ horizontal pairs.
3. Set a measurement probe with 10x attenuation; connect the probe to the RFQ vertical pair, and the ground probe to the RFQ horizontal pair
4. Place a toroid with several windings, of the probe cable, near the oscilloscope channel used to observe the HV pulse; this toroid prevents current from the EMS power supply flowing through the oscilloscope and causes interference to the current pulse operation.
5. Proceed with step 1- 5 in section F.3 (ensure that the current pulse rate matches the RFQ frequency as shown in Appendix D)
6. To observe the HV pulse, set the vertical axis of the oscilloscope screen to 50 V/div or 100 V/div, depending on the oscilloscope capability, and adjust the horizontal (time) axis to 100 ns/div.
7. Rotate the current knob of the EMS power supply half-way, switch the power on, and increase the voltage slowly. **CAUTION: Do not touch the RFQ device from this point on.**
8. During HV operation, observe the HV pulse appearing on the oscilloscope screen, and ensure the stability of both DC 60 V and EMS power supplies; please refer to measurement data on Appendix G. **NOTE**: Do not turn the voltage beyond 700 Vpp, seen from the oscilloscope, as higher voltage may damage the probe (rated for 670 Vmax).

9. To measure the temperature of components and the cooper heatsinks, place a probe on the measurement target immediately after turning off the power supplies, the switching control circuit, and the cooling fans. Measuring temperature during HV pulsing may cause interference.

APPENDIX G

Single-Polarity High-Voltage Pulsing Measurement Data

Table G1 below presents measurement data of single-polarity HV pulsing operation at 700 Vpp.

Table G1. High-Voltage Pulsing Data

RFQ Freq. [MHz]	Current Pulse Rate [kHz]	DC 60V current [A]		HV Pulsing			Time [ns]		Positive Width Duty Cycle [%]
		no HV	HV	EMS [V]	Vpp [V]	EMS [A]	Rise	Fall	
1	113	0.52	0.53	500	700	0.28	18.5	21.50	51.70
2	200	0.90	0.92	500	700	0.55	18.5	21.90	53.30
3	301	1.30	1.33	500	700	0.81	18.5	22.00	55.00

Table G2 below presents the temperature reading of several circuit components during HV pulsing at 3 MHz and 700 Vpp.

Table G2. Temperature Reading (°C) at 3 MHz and 700 Vpp

Room	18.6
FET heatsink (top)	49
FET heatsink (bottom)	44
APT1001RBN MOSFET	30
R gnd	66
R ems	47
R limiter	44

Note:
R gnd = power resistor connecting source (lower FET) and ground (EMS)

R ems = power resistor connecting drain (upper FET) and "+" (EMS)
R limiter = power resistor on the single primary wire (current pulse)

APPENDIX H

Recommendations for Double-Polarities High-Voltage Switching

Developing the current HV pulsing system with two polarities requires careful analysis involving the development of trigger circuit and current pulse controller, the power supply measurement for FET boards, and the development of double-polarities HV switching circuit.

H.1 Trigger Circuit and Current Pulse Controller

1. The first series module of two FET boards uses phase 1 for the low-side board, and phase 2 for the high-side board (see Fig. F2a and F2b). The second module will use phase 1 for the high-side board, and phase 2 for the low-side board.
2. Future development of trigger circuit and current pulse controller using FPGA or microcontroller will enable easy control of the RFQ rate and the current pulse rate, as well as timing adjustments.

H.2 FET Board Power Supply

1. A stack of four FET boards may share a single primary wire; however, experiments are needed to determine the power supply requirement and the current pulse rate.
2. Operating FET boards with higher DC voltage power supply than 60 V may increase the power dissipation of FET board components; therefore, measurements and more configurations may be needed.

H.3 Double-Polarities HV Pulsing

1. For double-polarities HV pulsing, a coaxial cable will deliver the conduction from the HV switching circuit to each of the RFQ axis. The outer conductors of each coaxial cable should be connected together to minimize inductance in the HV switching circuit.
2. Operating double-polarities HV pulsing is likely to increase the RFQ capacitive load by a factor of two; therefore, the current requirement from the switching power will increase as well.
3. Temperature measurement of the components during HV pulsing is recommended. The measurement procedure is explained in step 9 of section F.6 in Appendix F.
4. Each series module of two FET boards will use a high-voltage power supply (rated for 600 Vmin).
5. To observe the HV pulse, oscilloscope (with at least 10x attenuation capability) and measurement probes (rated for 800 Vmax) are required.
6. A careful analysis, involving cable selection, loop area minimization, and components lay-out, is needed to minimize the inductance in the HV switching circuit; this analysis needs to consider the space available for the RFQ electronics in TITAN's test cage.

APPENDIX I

RFQ Assembly Diagrams

The following figures show the RFQ assembly diagram for TITAN facility (courtesy of Hart Sprenger from the TITAN group).

H.S./JUNE 16/03

RFQ INSULATOR

- FOR TOLERANCES SEE PAGE 2
- QUANTITY: 4
- ALL DIMENSIONS IN (mm)
- TOLERANCES ON HOLE CENTERS ARE NON-ACCUMULATIVE (CHAIN DIM'S)

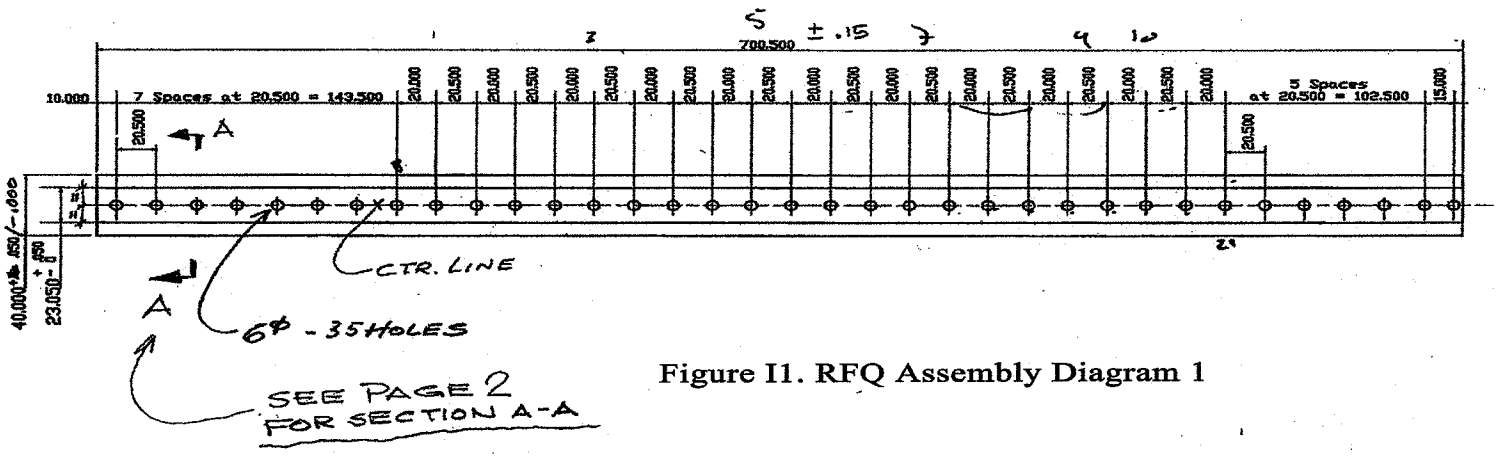


Figure I1. RFQ Assembly Diagram 1

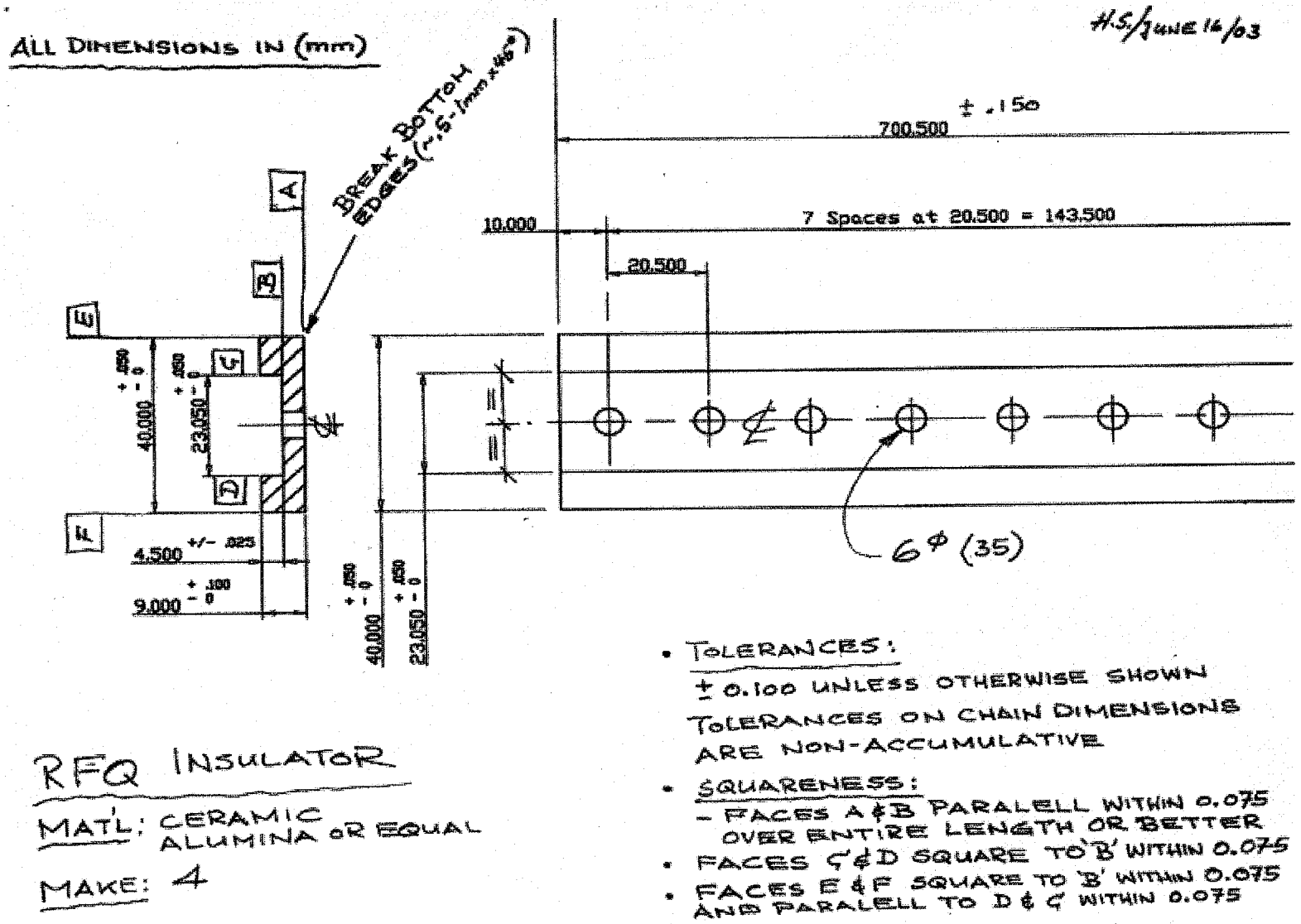


Figure I2. RFQ Assembly Diagram 2

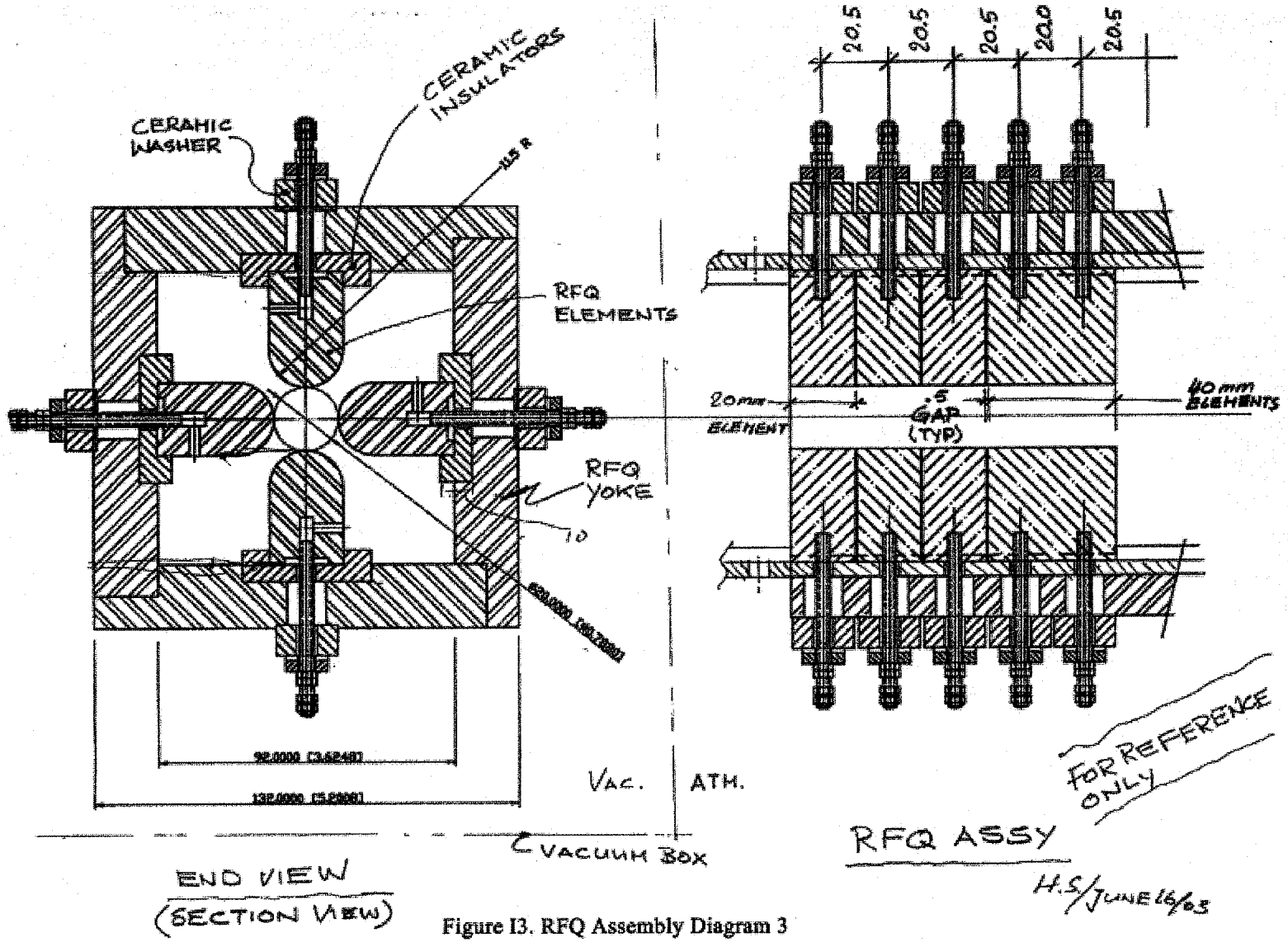


Figure I3. RFQ Assembly Diagram 3

APPENDIX J

RF Drive Electrical Configuration for TITAN's RFQ Beam Cooler and Buncher

Figure J1 shows the electrical configuration of the RFQ Beam Cooler and Buncher for TITAN facility (courtesy of Dr. Vaz from TITAN group).