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DESIGN NOTE
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CAPACITANCE OF TITAN RFQ DRIVER AND RFQ STRUCTURE, EXTRACTION ELECTRODE CONSIDERATIONS, AND POWER DISSIPATION IN THE DRIVER

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Abstract

The TITAN experiment employs a RF square wave RFQ Driver to perform 2-dimensional focusing of the ion beam within the RFQ, along a plane normal to the beam's intended trajectory, in an effort to confine ion motion along a stable path; hence the ions can be trapped and collected for extraction. This design note presents information about the distributed capacitance of the TITAN RFQ driver and RFQ structure. A comparison of predicted and measured values is provided. In addition this design note discusses the extraction electrodes. PSpice simulation results for power dissipation in various components are also presented.

I. RFQ DRIVER

The Radio Frequency Quadrupole (RFQ) driver for TITAN consists of two MOSFET modulators (Figure 1) for charging and discharging the four poles of a RFQ. Each modulator drives two opposite poles of the RFQ (Figure 2). Each modulator contains six MOSFET modules: in Figure 1 the MOSFETs are shown as switches with a parallel capacitor (C_{DS}) to represent the (non-linear) drain-source capacitance of the MOSFET. The top three and bottom three modules in each modulator form the "pull-up" (PUP) and "pull-down" (PDN) stacks, respectively. When the PUP (PDN) stack is turned on, proceeding turn-off of the PDN (PUP) stack, the voltage swing at each High Voltage (HV) output is equivalent to the supply voltage. This signal is fed to the RFQ via 50 Ω SHV cables (1 pF/cm) and SHV connectors mounted on the RFQ tank (4.66±0.12 pF (at 1MHz) per connector). From the HV connector, the signal is coupled to the RFQ poles via a series connected coupling capacitor (Crf in Figure 2).

The voltage swing on a pole, during charging and discharging, is equal to the supply voltage. The poles are charged (discharged) from their bias level minus half the supply voltage to their bias level plus half the supply voltage, and then discharged to their bias level minus half the supply voltage. In Figure 1, the sum of the DC supply voltages DC+ and DC– must not exceed 1 kV.

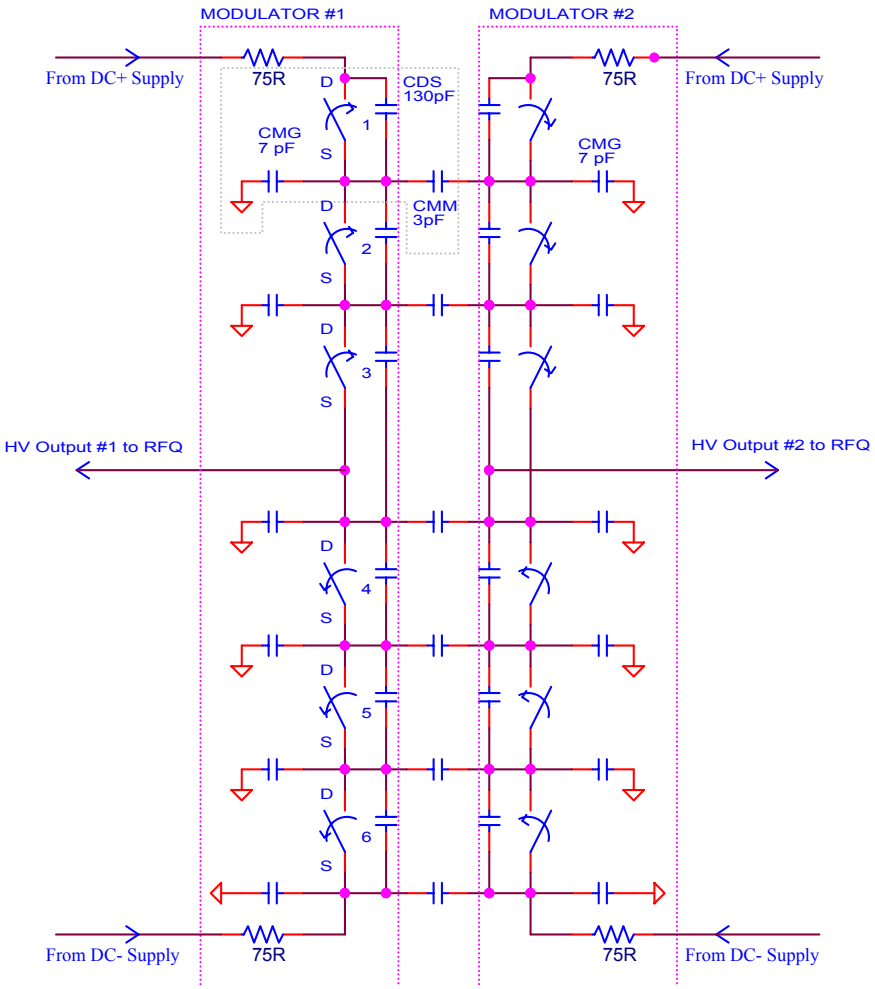

Figure 1: Electrical model of RFQ driver

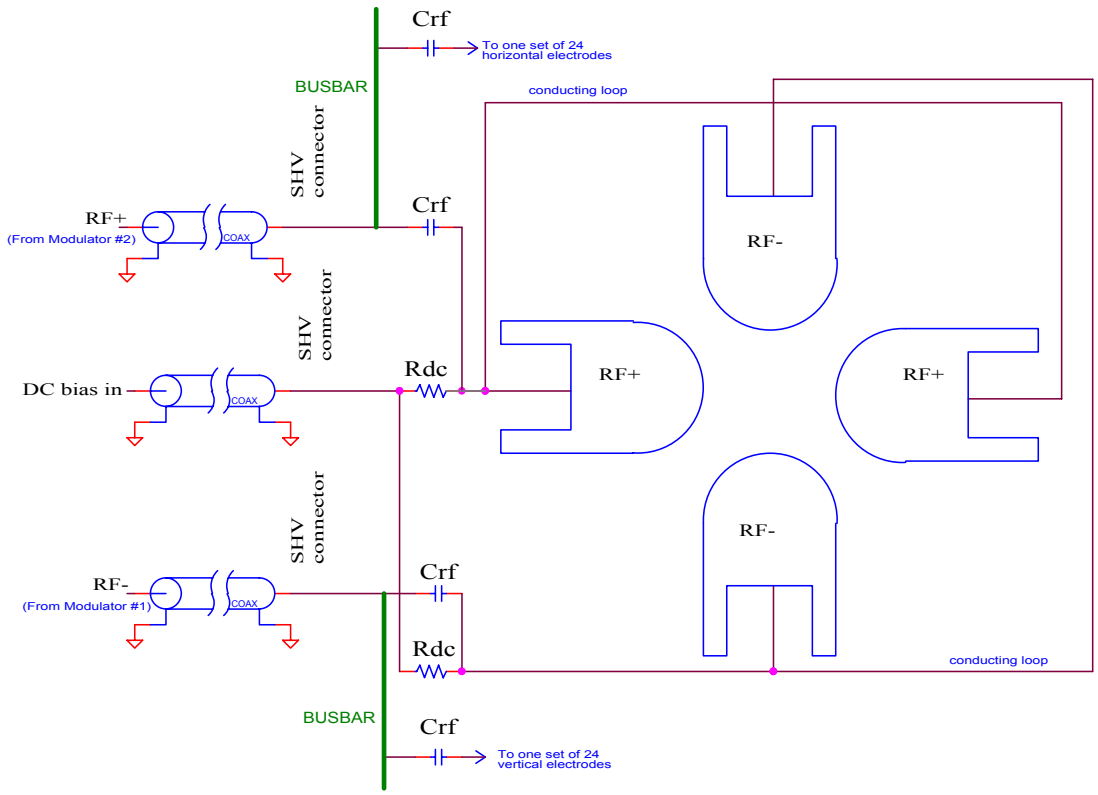

Figure 2: Cross-sectional view of 4 RFQ electrodes, their DC biasing and pulse coupling arrangement – this figure applies to all RFQ electrodes except for the extraction electrodes.

A simplified electrical model of the RFQ driver is shown in Figure 1. Each module has a voltage dependent drain to source capacitance (C_{DS}) associated with its DE375-102N12A FET, a capacitance from its source to ground (C_{MG}), and an inter-module capacitance (C_{MM}). Results from Coulomb [3] simulations indicate a capacitance to ground of approximately 7 pF per module and a capacitance of 3 pF per module between modules of adjacent stacks (C_{MM}). However these simulations neglect the primary winding of the ferrite transformers, which is known to add between 0.8 pF/module and 2 pF/module to ground, depending upon the position in the stack [1]: lumping 1 pF/per module with the predicted 7 pF per module to ground gives a value of 8 pF for C_{MG}. The MOSFETs exhibit a temperature dependent on-state resistance between 1 Ω and 2 Ω [2]. The stacks are driven anti-phase and the on-state stack is always turned off prior to the other stack turning on in order to avoid cross conduction [2].

The effective capacitive load $\left(=2\times\frac{E}{V^2}\right)$ to ground of an off-state stack is calculated from the energy (E) required to charge the capacitance to voltage V. The effective load capacitance consists of:

- the effective DS capacitance of the off-state stack (C_{DS3});
- the effective module to ground capacitances (C_{MG});
- the effective capacitance between modules of adjacent stacks (C_{MM}).

The voltage that the source of module 3 swings through is equivalent to the supply voltage (V), whereas the sources of modules 2 and 4 and modules 1 and 5 swing through approximately two thirds and one third of the supply voltage, respectively [2]. The source of module 6 is at potential

DC– and therefore its source potential is assumed to be constant. The effective capacitance to ground (C_{EFM2}) of the two modulators, has been calculated using PSpice. C_{MG} was set to 8 pF and C_{MM} was firstly set to 3 fF and subsequently to 3 pF. C_{MM} was then set to 3 pF and C_{MG} was firstly set to 8 fF and then subsequently to 8 pF. In both cases the predicted power supply current was used to determine the effective capacitance due to C_{MG}.

$$C_{EFM2} = \left(3.9C_{MG} + 7.5C_{MM}\right) \tag{1}$$

Hence, if C_{MG} = 8 pF and C_{MM} = 3 pF, then C_{EFM2} = 54 pF for the two modulators (27 pF per modulator). From equation (1), it is evident that reducing C_{MM} by 1 pF has almost twice the effect on C_{EFM2} of reducing C_{MG} by 1 pF.

Similarly PSpice was used to determine the effective capacitance (C_{EFM1}) for the test condition when the DC terminals of one modulator are grounded:

$$C_{EFM1} = \left(1.85C_{MG} + 1.77C_{MM}\right) \tag{2}$$

Hence, if C_{MG} = 8 pF and C_{MM} = 3 pF, then C_{EFM1} = 20 pF.

II. RFQ STRUCTURE

The RFQ structure (Figure 3) embodies 4 stainless steel poles. Each pole consists of 24 electrodes, separated by 0.5 mm air gaps, and the pole length spans 0.7 m. The shortest electrodes are 8 mm long, and the longest electrodes are 40 mm long. Electrical isolation between adjacent electrodes is necessary for independently assigning DC potentials to the electrodes in order to form the trapping potential. Each pole's 24 electrodes are secured to a U-shaped ceramic insulator (Figure 3). In the present design the four insulators are secured to three stainless steel support frames (Figure 3) attached to the RFQ box's lid: the support frames are at ground potential. The ceramic insulator is used to electrically isolate the electrodes from the supporting yoke, which is at ground potential.

The output from a modulator is connected to a hermetically sealed SHV connector on the RFQ tank using a SHV cable: a wire connected to a conducting push pin, that is in mechanical contact with the SHV connector, relays the signal present at the SHV connector to a conducting bus bar that spans the length of a pole (Figure 2). There are 2 bus bars: one for each set of opposite poles (Figure 2). One lead of each coupling capacitors (C_{rf}), 48 in total, is connected to the busbar and the other lead connects to an electrode pertaining to one of two opposite poles (Figure 2). Conductor loops connect opposite electrodes of the horizontal poles; also conductor loops connect opposite electrodes of the vertical poles (Figure 2). Hence only one busbar is required for the pair of horizontal poles, and one busbar for the pair of vertical poles. A DC coupling resistor (Rdc in Figure 2) connects from each set of horizontal electrodes to an SHV connector: similarly a DC coupling resistor also connects from each set of vertical electrodes to an SHV connector (Figure 2). DC bias is applied from one SHV connector to both a horizontal set and vertical set of electrodes (Figure 2): hence there are 24 SHV connectors for applying DC bias. A cross sectional view of four RFQ electrodes showing the pulse coupling and DC biasing arrangement is provided in Figure 2.

Each coupling capacitor (C_{rf} in Figure 2) is a "Panasonic series KBP capacitor" rated at 2 kV DC [7]. The value of the coupling capacitor is 220 pF for the 2 extraction electrodes and 5.6 nF for each of the other 22 electrodes per pole.

The DC coupling resistors for all the electrodes, except the 2 extraction electrodes, are manufactured by the Japan Hydrazine Company, type RG, rated at 750 V DC and 0.25 W [8]: their value is 10 MΩ each.

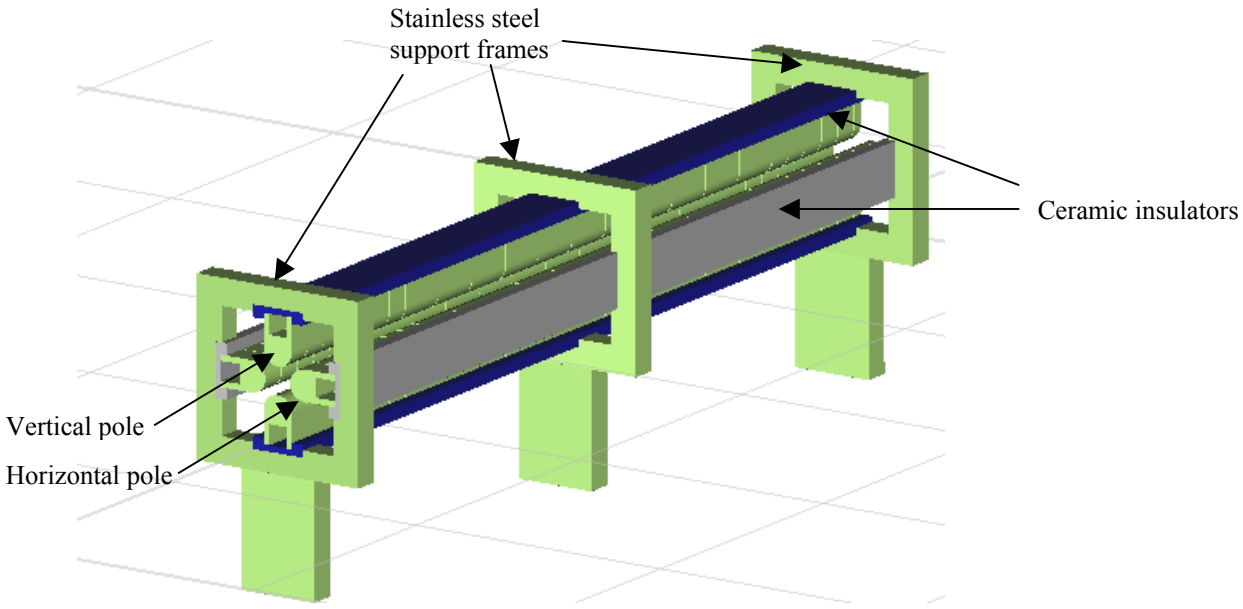

Figure 3: RFQ structure showing 4 poles, ceramic insulators (vertical poles in blue, horizontal poles in grey), and window frame supports.

EFFECTIVE CAPACITANCE

Table 1 lists six tests that were conducted in order to determine the distributed capacitance of the RFQ driver and the RFQ structure (the DC bias input of the RFQ was left floating for these measurements). During each test the average current from the 400 V power supply was measured: this current corresponds to charging the capacitance shown in the third and fourth columns of Table 1. In order to measure average current, an RC network (0.575 Ω in parallel with 300 nF) was placed inline with the positive supply terminal feeding both modulators. The voltage measured across the known resistance of 0.575 Ω was used to calculate the average current drawn from the supply: care was taken to check that the temperature of the 0.575 Ω resistor remained more or less constant.

In Table 1:
C_{DS3} is the linearized drain to source capacitance of 3 series, off-state, DE375-102N12A MOSFETs;
C_{CABLE_LHS} is the capacitance of the SHV cable from modulator #1 (LHS modulator, as viewed from the front);
C_{CABLE_RHS} is the capacitance of the SHV cable from modulator #2 (RHS modulator, as viewed from the front);
C_{VG} is the total capacitance from the 2 vertical poles of the RFQ to ground;
C_{HG} is the total capacitance from the 2 horizontal poles of the RFQ to ground;
C_{HV} is the total capacitance from the 2 horizontal poles of the RFQ to the 2 vertical poles;
C_{EFM2} is the total effective capacitance of the 2 modulators.

The total effective capacitance of both the modulators & RFQ, C_{EF} (equation 3), was derived based on the charge that the power supply must deliver to each constituent of the capacitance per cycle.

$$C_{EF} = 4C_{DS3} + C_{CABLE\_LHS} + C_{CABLE\_RHS} + C_{VG} + C_{HG} + 4C_{VH} + C_{EFM2} \quad (3)$$

From Test #1 of Table 1 the measured capacitance is 590 pF for the RFQ driver. The calculated effective capacitance to ground of the modulator, due to parasitic capacitances, is 54 pF (equation 1): hence $4C_{DS3}$ = 590 pF−54 pF = 536 pF. From reference [2] the effective capacitance of a DE375-102N12A MOSFET is approximately 390 pF with 133 V across it. Hence 3 series DE375-

102N12A MOSFETs, with a total of 400 V equally distributed between the MOSFETs, would have a capacitance (C_{DS3}) of approximately 130 pF. Therefore 4 stacks of MOSFETs have a total effective capacitance (4*C_{DS3}) of 520 pF; which is in good agreement with the 536 pF derived from the measurements in Table 1.

The equations in Table 1 have been solved (using the measured values of capacitance together with C_{EFM2} = 54 pF and C_{EFM1} = 20 pF) for each constituent of the capacitance: the results are shown in Table 2.

Table 1: Measurements carried out on TITAN RFQ and driver and corresponding capacitance value.

Test Number	Configuration for Test	Corresponding Capacitance from Measurement	Capacitance derived from measured current
1	Both modulators operated without SHV cables (i.e. no connection at outputs).	$4C_{DS3} + C_{EFM2}$	590 pF
2	Left hand side modulator operated with its output connected to its SHV output cable: the other end of this SHV cable is not connected. Both DC terminals of the right hand modulator are grounded.	$2C_{DS3} + C_{CABLE\_LHS} + C_{EFM1}$	342 pF
3	Right hand side modulator operated with its output connected to its SHV output cable: the other end of this SHV cable is not connected. Both DC terminals of the left hand modulator are grounded.	$2C_{DS3} + C_{CABLE\_RHS} + C_{EFM1}$	336 pF
4	Both modulators connected to the RFQ's SHV RF connectors via their SHV cables. Left hand side modulator operated. Both DC terminals of the right hand modulator are grounded.	$2C_{DS3} + C_{CABLE\_LHS} + C_{VG} + C_{VH} + C_{EFM1}$	633 pF
5	Both modulators connected to the RFQ's SHV RF connectors via their SHV cables. Right hand side modulator operated. Both DC terminals of the left hand modulator are grounded.	$2C_{DS3} + C_{CABLE\_RHS} + C_{HG} + C_{VH} + C_{EFM1}$	615 pF
6	Both modulators operated with output cables connected to the RFQ.	$4C_{DS3} + C_{CABLE\_LHS} + C_{CABLE\_RHS} + C_{VG} + C_{HG} + 4C_{VH} + C_{EFM2}$	1503 pF

Table 2: Breakdown of overall effective capacitance for the RFQ driver and structure

	Value (pF)	% of total
4*C_{DS3}	536	35.7
C_{CABLE_LHS}	54	3.6
C_{CABBLE_RHS}	48	3.2
C_{VG}	170.5	11.3
C_{HG}	158.5	10.5
4*C_{HV}	482	32.1
C_{EFM2}	54	3.6
TOTAL (C_{EF})	1503	100

Table 2 shows that $4C_{DS3}$ and $4C_{HV}$ constitute, between them, almost 70% of the overall effective capacitance of the RFQ structure and driver. Recommendations for reducing C_{DS3} are given in section IV. Reduction of C_{HV} can be achieved by replacing the conducting loops (Figure 2) with two additional RF busbars and AC coupling capacitors. Shortening the pole length, and increasing the size of the aperture between the four poles would result in the requirement of a higher RF focusing potential and therefore would most likely increase overall power dissipation.

3D simulations of the RFQ have been carried out using Coulomb [3]: these simulation results were used as a basis for modifying the original RFQ structure. Originally, the yoke supporting the ceramic insulator, used to electrically isolate the electrodes from the supporting yoke at ground potential, was a solid stainless steel bar spanning the pole length (Figure 4). As indicated in row five of Table 3, the solid yoke design presented 491 pF of additional effective capacitance to ground (i.e. 2*410 pF – (170.5 pF + 158.5 pF)) when compared to the present design (three 19 mm long window frame supports). This solid support yoke therefore implies that the total power consumption and RFQ rise/fall times would be increased by almost 33%, relative to the current design. This is a conservative estimate since the 410 pF to ground for either set of poles doesn't account for the added capacitance to ground that would have been introduced due to the addition of the conducting loops connected between opposite poles.

Efforts to minimize the capacitive load presented by the RFQ structure included:

- modifying the supporting yoke structure to consist of three 19mm thick stainless steel window frame supports;
- reducing the length of the screw threads that hold the electrodes in place, and milling out the electrodes thereby increasing the height of their feet from 2mm to 10mm. Milling out the electrodes also significantly reduces the weight of the structure, thereby reducing the mechanical stress on the ceramic insulators.

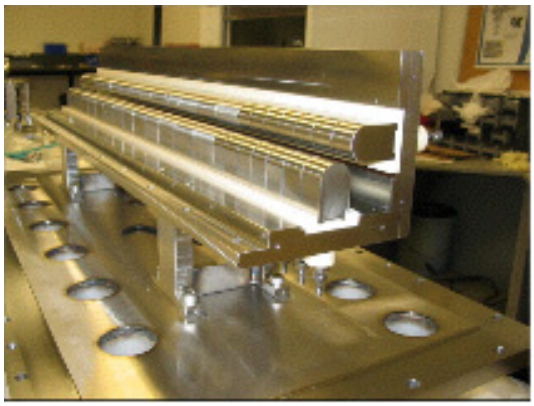

Figure 4: RFQ structure with solid bar supporting insulating ceramic and electrodes.

To date Coulomb simulations, to predict capacitance for the RFQ structure, did not include the RF busbars and RF coupling capacitors: adding the missing elements into the simulation will increase the predicted values for the capacitances from the horizontal and vertical rod sets to ground (C_{HG} and C_{VG}). In addition the conducting loops connecting opposite electrodes were modeled as two-dimensional surfaces with a 2 mm width rather than 3D conductors.
Measurements were carried out with the RFQ structure outside its box and aluminium foil was attached to one of its rectangular sides to simulate the effect of a ground plane.

Measurements shown in Table 3 suggest that the capacitive contribution from the RF busbar, RF coupling capacitors, and the wire loops is approximately:

- 40.5 pF (120.5 pF-80 pF) to C_{VH};
- 60.5 pF (170.5 pF-110 pF) to C_{VG};
- 48.5 pF (158.5 pF-110 pF) to C_{HG};

Hence, from equation 3, the total contribution of the RF busbar, RF coupling capacitors, and the wire loops to C_{EF} is approximately 271 pF (18% of the total measured capacitance of 1503 pF).

Table 3: Distributed capacitance values of RFQ structure.

Comment	C_{VG} (pF)	C_{HG} (pF)	C_{VH} (pF)	Components modeled
Predicted (a)	20	20	75	Box, floating poles (no support structure) with electrodes as per original design (2 mm legs), ceramic insulator.
Predicted (b)	415	415	65	Box, poles with electrodes as per original design (2 mm legs), ceramic insulator, original **solid yoke** support.
Predicted (c)	70	70	75	Box, poles with electrodes as per original design (2 mm legs), ceramic insulator, **3 of 19 mm long window frame** supports attached to lid.
Predicted (d)	91	87	116	Box, poles with modified electrodes design (10 mm legs), ceramic insulator, 3 of 19 mm window frame supports attached to lid, **2D wire loops** (surface conductors rather than volume conductors).
Measured (as per b)	410	410	not measured	Poles with original electrodes design (2 mm legs), ceramic insulator, original solid yoke support attached to lid, long screws.
Measured	110	110	80	Poles with modified electrodes design (10 mm legs), ceramic insulator, window frame supports attached to lid, long screws
Measured (as per d)	170.5	158.5	120.5	Aluminium foil to simulate box ground plane along one rectangular side of RFQ, poles with modified electrodes design (10 mm legs), ceramic insulator, window frame supports attached to lid, wire loops connecting electrodes of opposite poles, 2 busbars, coupling capacitors, 21 DC biasing resistors (0.16 pF/resistor).

EXTRACTION ELECTRODES

Magnitude of RF Extraction Voltage

For 22 of the 24 electrodes the RF coupling capacitor value is 5.6 nF: this value is very large compared with the effective electrode capacitance and therefore the magnitude of the RF voltage, on these 22 electrodes, is almost equal to the magnitude of the applied RF voltage. However, the 2 extraction electrodes have a significantly smaller value of coupling capacitor: a reduced value is necessary for achieving the rise time of the RF bias voltage on the extraction electrodes (see equation 5). The magnitude of the RF voltage (V_{RF_ext}) on the extraction electrodes is given by:

$$V_{RF\_ext} = V_{RF}\left(1-\left(\frac{(2*C_{HV\_end}+C_{SHV}+C_{HG\_end})}{C_{RF\_ext}+(2*C_{HV\_end}+C_{SHV}+C_{HG\_end})}\right)\right) \quad (4)$$

Where:

- V_{RF} is the magnitude of the applied RF voltage;
- C_{SHV} is the capacitance of SHV connector (approx. 5pF);
- $C_{HG\_end} = C_{VG\_end}$: these represent the capacitance to ground of the horizontal or vertical extraction electrodes, respectively (each estimated to be 7 pF);
- C_{HV_end} is the capacitance between the horizontal extraction electrode and vertical extraction electrode ($2*C_{HV\_end}$ estimated to be 12 pF);

Hence $(2*C_{HV\_end} + C_{SHV} + C_{HG\_end})$ is estimated to be 24 pF.

Rise/Fall Time of Extraction Voltage

Twenty-two of the 24 electrodes have a DC bias level applied. The extraction voltage of the extraction electrodes is pulsed, on a relatively long time scale; the required rise-time of the extraction voltage on the extraction electrodes is 10 μs. Assuming that the output of the McGill pulser traverses between 0 V and V_{McG_ext}, the 10% to 90% rise and fall time of the extraction voltage (T_{ext}) is given approximately by:

$$T_{ext} = 2.2 * R_{dc\_ext} * C_{ext} \tag{5}$$

Where R_{dc_ext} is the value of the DC coupling resistor for the extraction electrode, and C_{ext} is the total effective capacitance of the extraction electrodes, as viewed from the McGill pulser input to the extraction electrode (Figure 5).

The total effective capacitance of the extraction electrodes (approx. 24 pF), to be driven by the McGill pulser, is given by the sum C_{SHV}, C_{HG_end}, $2*C_{HV\_end}$ and the value of the RF coupling capacitor for the extraction electrodes [C_{RF_ext}] (approx. 220 pF): the RF modulator output represents a virtual ground to the extraction voltage pulse.

The value of the RF coupling capacitor for the extraction electrodes dominates the effective capacitance of the extraction electrodes, hence the effective capacitance does not depend strongly upon whether the DC coupling resistors for the 2 extraction electrodes are inside or outside the vacuum tank.

The original design of the RFQ used a DC coupling resistor of 14 kΩ for the 2 extraction electrodes. During testing these resistors were observed to get very hot. Cooling of the DC coupling resistors for the extraction electrodes would be a problem in vacuum. Hence it is preferable to design for these resistors to be outside the vacuum: they are therefore shown this way (to the left hand side of the SHV connector) in Fig. 5.

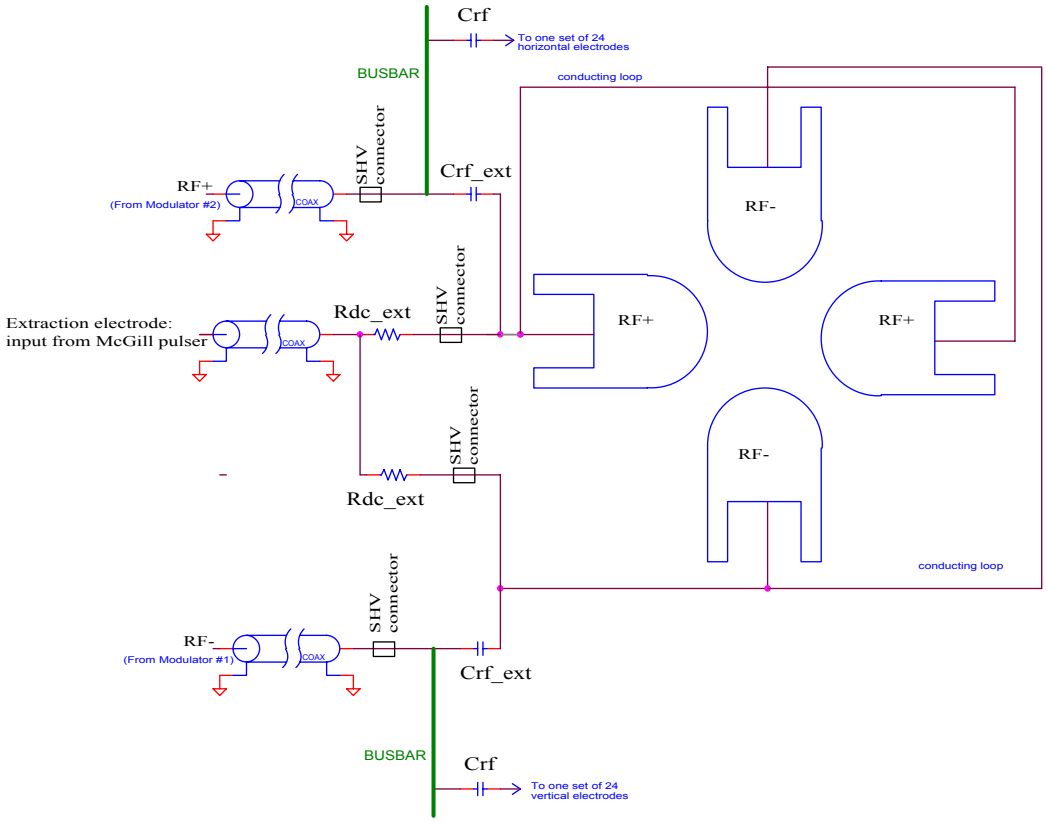

Figure 5: Cross-sectional view of 4 RFQ electrodes, their DC biasing and pulse coupling arrangement (for one of two sets of extraction electrodes).

In order to ensure a dissipation in the DC coupling resistors, for the 2 extraction electrodes, of not more than 1 W, at 400 V RF and 50% duty cycle, the value of this resistor must be at least 81 kΩ. The resulting rise/fall time of the extraction voltage, assuming C_{RF_ext}=220 pF, is approximately 43 µs, which is longer than the required 10 µs.

Table 4 shows the ratio V_{RF_ext}/V_{RF}, derived from equation 4, and the rise time of the extraction voltage as a function of both R_{dc_ext} and C_{RF_ext}. Achieving a rise time of approximately 10 µs, for the extraction voltage, with R_{dc_ext}=81 kΩ requires a value of C_{RF_ext} of approximately 33 pF; however only 58% of the RF voltage is expected to couple through to the extraction electrodes. Two alternative approaches can be used:

- Reduce the value of R_{dc_ext}, e.g. to 40.5 kΩ, either by paralleling higher value resistors or connecting lower value resistors in series; the power dissipation is shared between the resistors.
- Modify the McGill extraction voltage pulse to have two discrete non-zero levels during extraction. For example, for R_{dc_ext}=81 kΩ and C_{RF_ext}=220 pF, in order to achieve an extraction voltage of magnitude V_{McG_ext} on the extraction electrodes in a time (t) of 10 µs, then the initial output voltage of the McGill pulser (V_{McG}) is given by:

$$V_{McG} = \frac{V_{McG\_ext}}{\left(1 - e^{-\left(t/T_{ext}\right)}\right)} = \frac{V_{McG\_ext}}{\left(1 - e^{-\left(10\,\mu s/(81k\Omega*(220\,pF+24\,pF))\right)}\right)} = \frac{V_{McG\_ext}}{0.397} \qquad (6)$$

i.e. the initial pulse voltage, from the McGill, is initially approximately 2.5 times greater than the required extraction voltage on the extraction electrodes, for 10 μs, and then the McGill pulser voltage reduces down to V_{McG_ext}.

Table 4: ratio V_{RF_ext}/V_{RF}, derived from equation 4, and the rise time of the extraction electrode extraction voltage, derived from equation 5, as a function of both R_{dc_ext} and C_{RF_ext}.

R_{dc_ext} (Ω)	C_{RF_ext}	V_{RF_ext}/V_{RF}	$T_{ext}(=2.2*R_{dc\_ext}*C_{ext})$ (based on a McGill pulser with levels of 0 V and V_{McG_ext})
500 k	220 pF	0.90	268 μs
81 k	220 pF	0.90	43.5 μs
81 k	100 pF	0.81	22.1 μs
81 k	47 pF	0.66	12.7 μs
81 k	33 pF	0.58	10.2 μs
40.5 k	220 pF	0.90	21.7 μs
40.5 k	100 pF	0.81	11.0 μs

IV. POWER CONSIDERATIONS

The effective capacitance as "seen" by the power supply can be determined from the average current, *Iavg*, being supplied at voltage V_{SUPPLY} (equation 7). Current limiting for both charging and discharging currents is achieved using inline resistance of 75 Ω connected from the DC+ and DC- (Figure 1) terminals to the power supply lines. The 75 Ω resistance presently comprises two series resistors of type 886SP from Kanthal Globar [4]. Each type 886SP resistor is 5" long by 0.75" outside diameter; Kanthal Globar rates these resistors at 90 W average power dissipation at an ambient temperature of 40°C. The maximum allowable temperature of the resistors is 350°C.

At 400 kHz (f_{RFQ}) and 400 V DC supply voltage (V_{SUPPLY}), an average current (*Iavg*) of 240 mA is drawn from the DC supply to drive the present RFQ (3 window frame supports). From equation (7), the effective capacitance, $C_{EF,}$ being driven is 1503 pF.

$$Iavg = C_{EF} \times V_{SUPPLY} \times f_{RFQ} \tag{7}$$

The power from the 400 V supply is the product of the current and voltage. The majority of this energy is dissipated in the MOSFETs and 4 sets of 75 Ω resistance connected inline with the DC supply lines. PSpice simulations predict that approximately 83% of the power, from the power supply, is dissipated in the four sets of 75 Ω resistors: each set of resistors dissipates approximately 21% of the total power consumed from the supply. Approximately 17% of the power, from the power supply, is dissipated in the 12 MOSFETs. However the dissipation in each MOSFET is not equal: the dissipation in the MOSFETs at the pulse end of the stack is approximately twice that dissipated in the MOSFETs at the DC end of the stack.

The unequal power dissipation in the MOSFETs is due to the following:

- the parasitic capacitances from each module to ground (C_{MG}) and from module to module (C_{MM}) are relatively high;

- Fast grading capacitors [2] are not connected across the drain-source of the MOSFETs.

The net effect of the relatively high parasitic capacitance and the absence of fast grading capacitors is to cause non-ideal voltage grading in the stack. For example, in the ideal case each of the MOSFET would support 33.3% of the DC supply voltage; however PSpice simulations show that the MOSFET at the pulse end of the stack supports approximately 40% of the voltage.

The energy required to charge the effective capacitance to voltage V is equal to the energy dissipated in, for example, the PUP side 75 Ω resistors throughout the charging period; the energy stored in the effective capacitance is then dissipated in the PDN side 75 Ω resistors during the discharge period. Hence the value of energy, per pulse, given by (equation 8) is equal to half of the energy consumed, per charge-discharge cycle, from the power supply.

$$E = \frac{1}{2} C_{EF} (V_{SUPPLY})^2 \tag{8}$$

The average power delivered (P_{ps}) by the power supply is directly proportional to f_{RFQ} and proportional to V^2 (see equation 9).

$$P_{ps} = 2\left(\frac{1}{2} C_{EF} (V_{SUPPLY})^2 \times f_{RFQ} \right) \tag{9}$$

Table 5 shows the expected power consumption from the power supply, dissipation in the 75 Ω resistors, and dissipation in the MOSFET at the pulse end of the stack as a function of frequency and power supply voltage.

To minimize lifetime degradation of the DE375-102N12A MOSFETs it is necessary to keep their junction temperature well below the maximum rating of 175°C [6]. A target junction temperature of 100°C has therefore been chosen. The DE375-102N12A MOSFET is an RF avalanche rated device with a drain-source (D-S) rating of 1 kV and a power rating of 220W at a case temperature of 100°C [6]. The data sheet specifies a thermal impedance of 0.35°C/W [6] from the device's junction to a heat sink mounted to the device's planar conducting surface; hence sufficient cooling must be provided to ensure that the heat sink temperature does not exceed 73°C with a dissipation of 76 W in the MOSFET. This heat sink temperature corresponds approximately to a 45°C rise above an ambient of 30°C.

Table 5: expected power consumption from the power supply, dissipation in the 75 Ω resistors, and dissipation in the MOSFET at the pulse end of the stack (3 high stack) as a function of frequency and power supply voltage.

DC supply voltage (V_{SUPPLY}) (V)	Operating frequency (f_{RFQ}) (MHz)	Power from DC power supply (P_{ps}) (W)	Dissipation in each 75 Ω resistor (W)	Dissipation in MOSFET at pulse end of stack (W)
400	0.4	96	20	1.6
400	1.0	240	51	4.1
400	3.0	721	152	12.2
1000	0.4	601	126	10.1
1000	1.0	1503	316	25.4
1000	3.0	4509	947	76

Measurements of heat sink temperature rise above ambient have been carried out as a function MOSFET power dissipation and airflow [5]. A heat sink temperature rise of 45°C, for linear airflows of 500 fpm (feet per minute), 600 fpm, and 800 fpm in the vicinity of the fins of the heat sink, correspond to MOSFET power dissipations of 85 W, 95 W, and 170 W [5]. The thermal impedances from heat sink to air (R_{thHSA}) at linear airflows of 600 fpm and 800 fpm are 0.434°C/W and 0.262°C/W respectively [5], whereas in ambient air the thermal impedance is about 5°C/W. The measured airflow, across the MOSFET heat sinks, in the present configuration of the MOSFET driver and fans, is 800 fpm: hence the cooling of the MOSFETs should be adequate for operation at 1000 V and 3 MHz (see Table 3).

To maximize cooling of the tubular power resistors they should be placed such that minimal cross sectional area is normal to the air-flow (Figure 6). This configuration aids to improve the air-flow through the component as was confirmed for the tubular power resistors where the air-flow through the hollow inner diameter contributed significantly to the cooling of the resistor. Measurements of temperature vs. power dissipation at various airflows have not been made for the power resistors. This should be carried out as it may become significant at higher power consumptions where the resistance value may increase considerably if not adequately cooled.

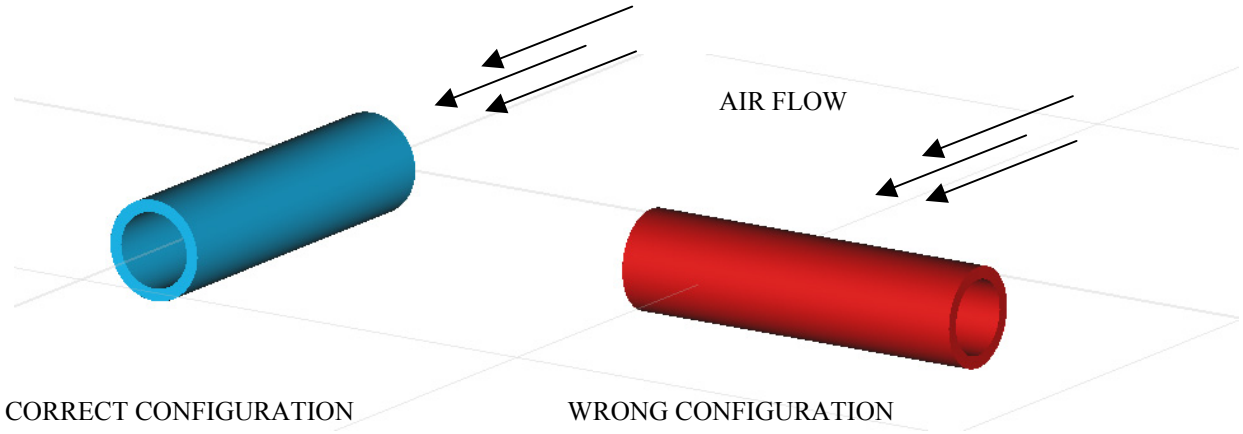

Figure 6: Component placement relative to direction of airflow from a cooling perspective

The power dissipation of a DC coupling resistor, equation (10), depends on its resistance, the supply voltage (V), and the duty cycle (duc) of the pulse voltage present at the electrodes. Table 6 shows the power dissipation of a 10 MΩ and an 81 kΩ DC biasing resistor for various duty cycles and voltages. A total of twenty-two 10 MΩ DC biasing resistors and two 81 kΩ biasing resistors on the extraction electrodes correspond to a total power dissipation of 2.2 W at 400 V and 50% duc.

$$P_{R_{DC}} = \frac{V^2}{R} \times duc \qquad (10)$$

The largest RMS current through a coupling capacitor pertains to those capacitors connected to the largest electrode (40 mm length). An RMS current of approximately 85 mA (210 mA) flows through the 5.6 nF capacitor associated with a 40 mm long electrode for 400 V (1000 V) and 3 MHz operation. Reference 7 shows the voltage rating of various "Series KBP 2 kVDC" capacitors as a function of frequency: extrapolating the curves up to 3 MHz gives a peak-peak voltage rating of approximately 50 V for a 5.6 nF capacitor: the predicted maximum pulse voltage across a 5.6 nF capacitor, associated with a 40 mm long electrode, for 1000 V operation is approximately 8 V. Extrapolating the curves of reference 7 up to 3 MHz gives a peak-peak voltage rating of approximately 150 V for a 220 pF capacitor. The predicted maximum pulse voltage across a 220 pF

capacitor, associated with a 19 mm long extraction electrode, for 1000 V operation is approximately 80 V.

Table 6: Power dissipations in 10 MΩ and 81 kΩ biasing resistors

duty cycle (%)	RF voltage	Power dissipation (mW) in R_{DC}=10 MΩ	Power dissipation (W) in R_{DC}=81 kΩ
10	400	1.6	0.2
10	600	3.6	0.4
10	800	6.4	0.8
10	1000	10	1.2
50	**400**	**8**	**1**
50	**600**	**18**	**2.2**
50	**800**	**32**	**4**
50	**1000**	**50**	**6.2**
90	400	14.4	1.8
90	600	32.4	4.0
90	800	57.6	7.1
90	1000	90	11.1

Recommendations for reducing power consumption are as follows:

1. Modify the modulator aluminium support structure to decrease the inter-module capacitance and the capacitance from the modules to ground. When doing so, attempt to preserve the current support structure's ability to direct the airflow towards the modules and power resistors.

2. Replace the conducting loops in the RFQ with two additional RF busbars.

3. Increase the number of MOSFET modules per stack from 3 to 4. This would reduce $4*C_{DS3}$ from 520 pF to approximately 460 pF. Further increasing the number of MOSFET modules per stack to 5 would reduce $4*C_{DS3}$ to 420 pF. However, when more MOSFET modules are added per stack, it will be necessary to include fast-grading components [2].

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