1.0 INTRODUCTION

TRIUMF is Canada's national laboratory for particle and nuclear physics. It is a member of the international subatomic physics community and strives to play an important role in the global quest for a clearer understanding of subatomic particles and the fundamental forces that drive the universe [1]. TRIUMF's Ion Trap and Nuclear science (TITAN) group is working in collaboration with the CPT (Canadian Penning Trap) group to develop a state-of-the-art Penning trap facility at TRIUMF to exploit the available high intensity beams of exotic nuclei at the ISAC (Ion Separator and Accelerator) facility as per the recommendation of the Canadian Subatomic Five Year Plan Committee (SFYPC) made in June, 2001 [2]. Such a system is used to measure the mass of exotic isotopes to a very high level of precision. Current systems of this type presently exist at the following facilities for exotic species: ISOLDE, CERN, Switzerland (ISOLTRAP); ATLAS, ANL, USA (CPT); in preparation: SHIP, GSI, Germany (SHIPTRAP); NSCL, MSU, USA (LEBIT); IGISOL, JYFL, Finland (JYFLTRAP) [2].

ISAC (exotic nuclei production facility) has the potential to be the leading on-line facility with the highest production yields [2]. The ability to reach the most exotic isotopes as well as the privilege to draw from the knowledge of existing trap systems, makes TRIUMF the prime location for a second-generation facility to conduct super accurate mass spectrometry.

How will science benefit from such a costly long-term initiative?

Accurate mass measurements serve as a testing ground for nuclear models and stimulate their further improvement. One such application involves testing the unitary property of the CKM matrix. Such a test would serve to limit certain extensions to the current Standard Model of elementary particles. Presently it is unknown whether the 2.2δ deviation from unity is do to the limited accuracy of experimental data or do to limitations of the current model. Such a deviation suggests that we are between 98- 99% confident that the observed discrepancy between theory and experiments is not accidental. Ergo the nuclear physics community is skepticle that current nuclear models tell the whole truth.

The layout of TITAN's facility (Figure 1) consists of four stages: RFQ Cooler and Buncher, EBIT charge breeder, velocity selector (m/q selection stage), and the Precision Penning trap. The separated continuous ion beam from ISAC is cooled and bunched using a gas-filled linear radio frequency quadrupole (RFQ) Paul trap. The ions are then injected into an Electron Beam Ion Trap (EBIT), where charge breeding via electron stripping takes place. The beam is then extracted and sent through an additional separation stage where contaminants (other charge states or isobars) are removed by using a Wien filter (m/q selection). The high purity beam is finally transferred into the Penning trap where the mass of the ion of interest is determined to within a forecasted precision of 10^{-10} [2].

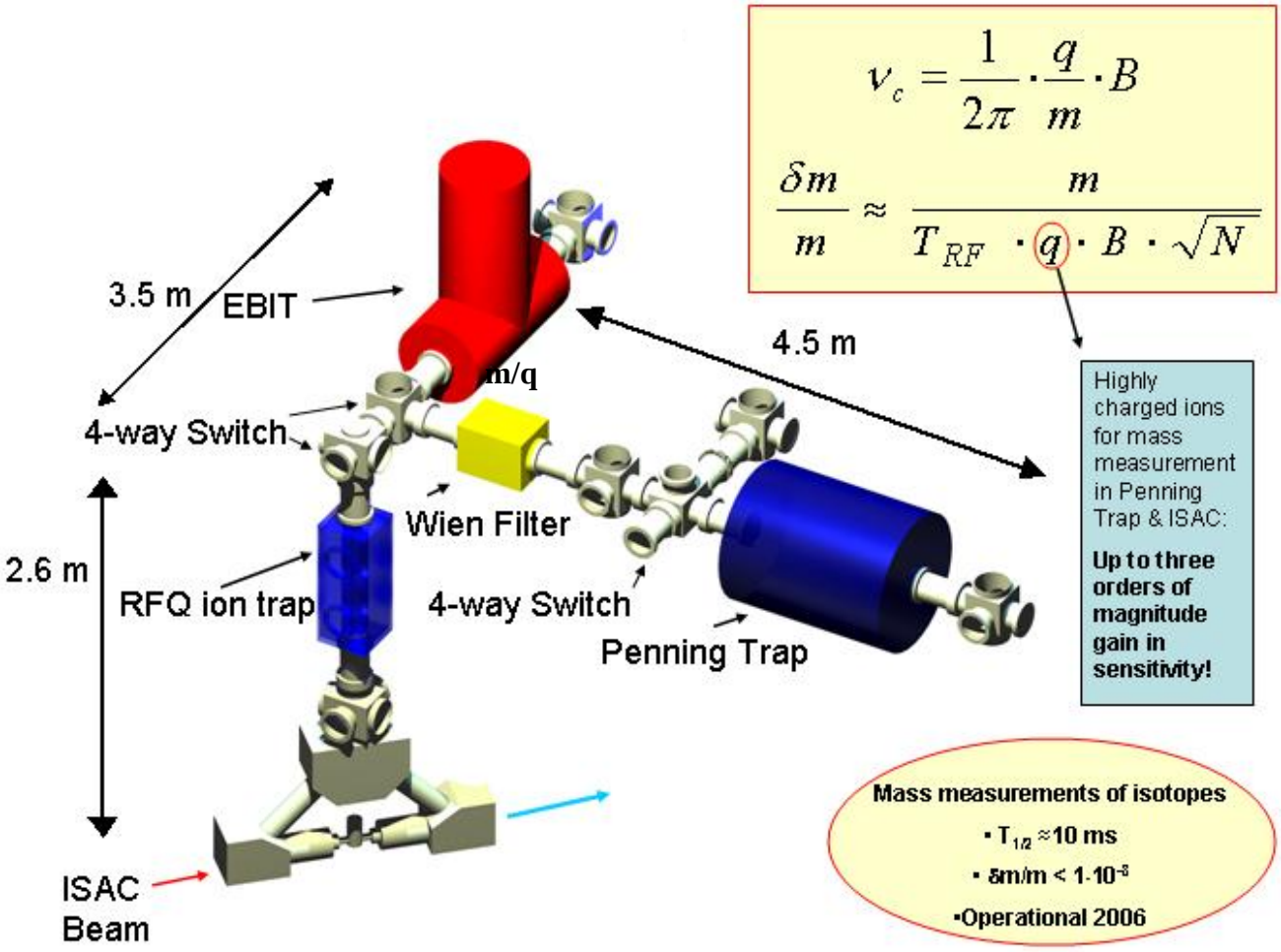

Figure 1. Layout of the TITAN system

If successful, the members of TITAN would become the pioneers of such high precision mass spectrometry conducted on isotopes whose half-lives are as short as 10msec.

How will TITAN achieve such precise mass measurements?

The factors governing the precision of the mass measurements made on a particular isotope inside the Penning Trap are: its mass (**m**), its half life ($\mathbf{T_{1/2}}$), its charge state (**q**), the strength of the Magnetic field (**B**) to which the ions are exposed, and the number of ions simultaneously within the trap (**N**). The precision is inversely proportional to **m**, and directly proportional to $\mathbf{T_{1/2}}$, **q, B, and** $\sqrt{\mathbf{N}}$. Nothing can be done about **m** and $\mathbf{T_{1/2}}$. Increasing **B** from approximately 6 Tesla to higher values is not financially practical, and the returns aren't substantial as one attempts to increase **N**. Therefore the only variable that can be controlled and provide significant increase in precision is **q**.

Other systems of this nature do not employ an EBIT to perform charge breeding hence the ions are usually singly charged. With the incorporation of the EBIT the ions can be positively charged from +20 to +30, thereby improving the precision by an equivalent factor. Prior to entering the EBIT the ion beam is cooled and bunched by the RFQ in order to enable fast and efficient charge breeding. The RFQ also reduces both the beam energy, to a value better suited for TITAN's precision mass measurements, as well as the energy spread of the beam [4].

The RFQ is made up of four segmented hyperbolic rods (Figure 2). A radio frequency (RF) electric field is applied to the rods in order to confine the ions in a two dimensional plane. The segmented rod structure allows for the application of an electrostatic field so as to confine the ions in the third dimension. Once trapped, the ions are cooled via interactions with an inert buffer gas such as Helium. The ions are then extracted from the trap in bunches.

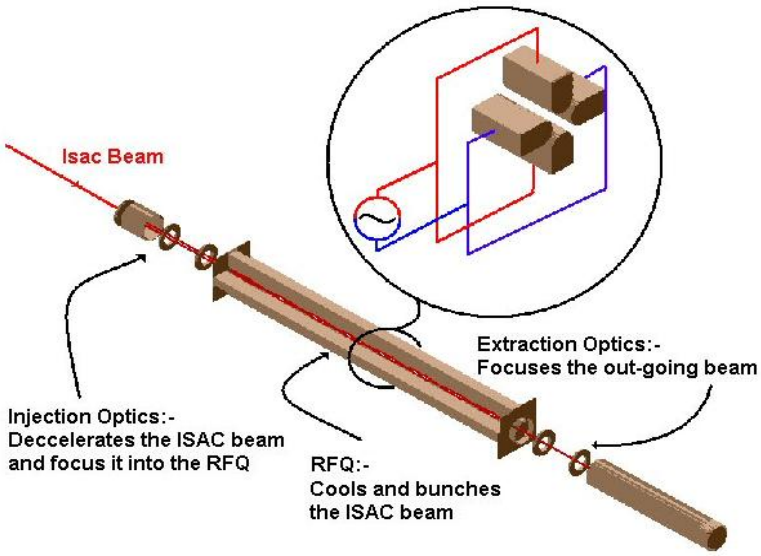

Figure 2. RFQ structure

The q-value [2], not to be confused with the charge state of the ions, governs the stability of the ion path in the RFQ and is directly and inversely proportional to the peak to peak amplitude and square of the angular frequency, respectively, of the RF signal. If the q-value does not remain within upper and lower thresholds defining its stability boundary, the ions will not be trapped. Lighter ions require higher frequency signals in order to be trapped; consequently, the peak to peak amplitude of the RF signal must be increased as well in order for the ion path to remain within the region of stability. This poses a great challenge in the design of the electrical system that will drive the RFQ since an increase in frequency and signal amplitude both lead to an increase in power consumption.

The scope of this report is limited to the scheme implemented to generate the RF signal providing two-dimensional focusing of the continuous ion beam inside the RFQ. The discussion commences with an outline of the specifications to be met by the High Voltage Radio Frequency Square Wave Generator (HVRFSWG) and follows with a system overview and a detailed description of its components. This includes the exposition of the theoretical underpinnings and the presentation and analysis of relevant data and observations. The conclusion extracts relevant

figures from the discussion and revisits the specifications to be met by the HVRFSWG in order evaluate the success of the project. Recommendations regarding further acquisition of pertinent data and system upgrades follow the discussion.

2.0 SYSTEM OVERVIEW

The HVRFSWG for TITAN's RFQ Ion Trap is an electrical system that generates two continuous square wave signals of opposite phase at RF frequencies up to 1 MHz with peak-to-peak amplitudes reaching 400V and rise/fall times that do not exceed 125nsec. This system is able to drive capacitive loads such as the RFQ.

2.1 HVRFSWG VS. OLD RFQ DRIVING TECHNOLOGY

Traditionally, RFQs are driven with a sinusoidal waveform utilizing RF amplifiers and ferrite cores for phase splitting. The bandwidth of such cores is quite limited and operation outside the region where the core's Q-factor is sufficiently high results in a significant portion of the energy being dissipated in the core. This causes the core to heat up and its magnetization curve to change thus leading to distortion of the sinusoidal waveform. Impedance matching networks are also required to match the system with its output load in order to prevent energy from being reflected back to the RF amplifier. The fact that one can only operate in a narrow frequency band, and do so at modest signal amplitudes limits mass measurements to heavier ions since lighter ions will not be trapped. To trap lighter ions (TITAN plans to trap ions as light as 11 a.m.u) one must be able to apply high amplitude/high frequency signals, and the HVRFSWG has the potential to do so.

2.2 SYSTEM LAYOUT

The HVRFSWG is housed within the RFQ Driver Rack – a cage like structure that is composed of a welded aluminum frame and mesh-like aluminum walls. The RFQ Driver Rack is secured on top of the RFQ lid in order to minimize cable lengths that are fed from the HVRFSWG to the HV connectors located on the RFQ lid (Figure 3).

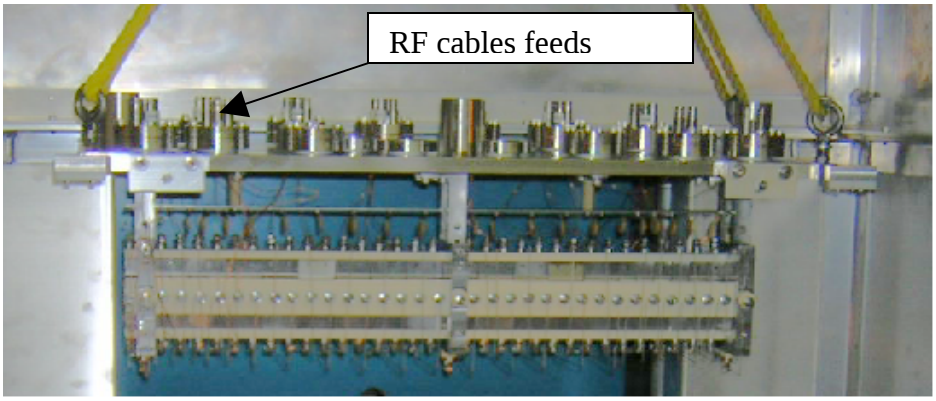

Figure 3. RF cable feeds on the RFQ lid.

The dimensions of the RFQ lid dictated the length (31.5") and width (14.5") of the rack whereas its height (18") was chosen to preserve sufficient clearance for crane access. The RFQ lid is the simply the top face of a rectangular stainless steel structure (box). There is a minimum clearance requirement of 8" from the Faraday cage (at earth ground potential) surrounding the RFQ box to the box itself. The RFQ box and Driver Rack float between 30 – 60 kV (HV ground) while the experiment is running.

The HVRFSWG's main components are: one MULAN Pulse Controller Board (MPCB), two Phase Driver Racks (PDRs) that can house a total of 16 1kV boards, one Power Supply Driver (PSD), and an INTERLOCK board. Michael Barnes and Gary Wait (KICKER group at TRIUMF) developed the MPCB, 1kV boards, PSD, and INTERLOCK board. The VME (Versa Module Europa) crate installed in the Blue HV cage provides the trigger signals necessary to drive the MPCB and PSD. Figure 4 shows a simplified block diagram of the HVRFSWG.

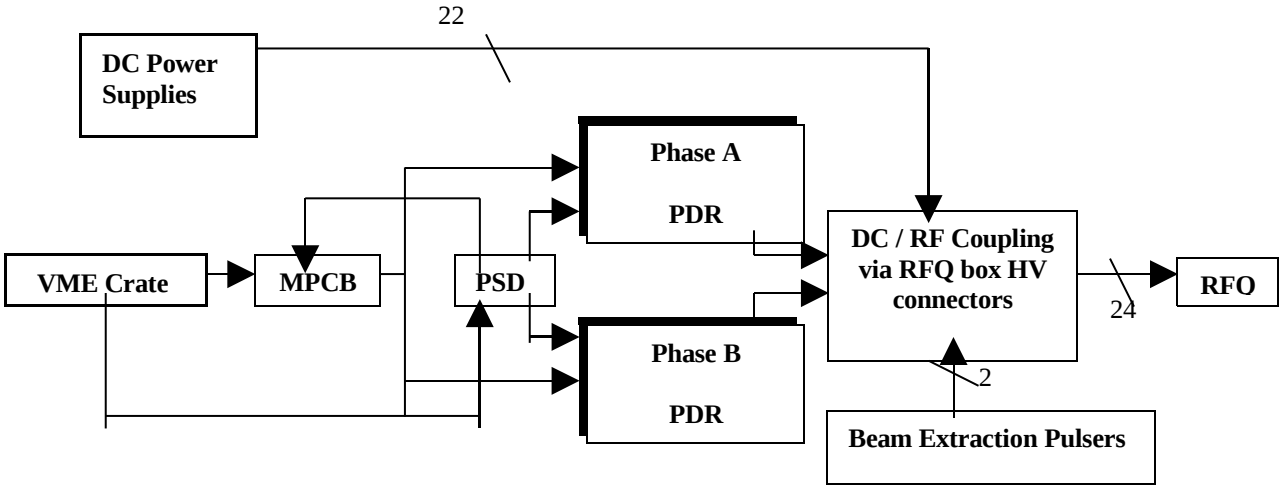

Figure 4. Simplified block diagram of the HVRFSWG.

3.0 MULAN PULSE CONTROLLER BOARD

The MPCB (Figure 5) can be operated in one of two modes – local and remote. In local mode (i.e. for lab testing) the MPCB internally generates PSD drive signal and this signal is fed to the PSD via a fiber optic transmitter on the MPCB. In remote mode, the DDS module inside the VME crate generates the PSD drive signal. This signal is fed to a fiber optic input on the MPCB via one of the fiber optic outputs of the squaring module that receives a sinusoidal input from the DDS module. As in local mode the signal is relayed to the PSD from a fiber optic transmitter on the MPCB.

The DDS also generate the RFQ driving signal. The frequency of this signal dictates the driving frequency of the RFQ. This sinusoidal signal serves as second input to the squaring module whose output is fed to the MPCB via a LEMO connector. From this signal, the MPCB generates two square wave signals of opposite phase (Φa and Φb). These two signals drive two sets, one

set per phase, of fiber optic HFBR-1528 transmitters. The two RFQ drive signals and the PSD drive signal are monitored using an oscilloscope via onboard LEMO connectors labeled "PULL UP", "PULL DOWN", and "PWR FREQ" respectively (Figure 5).

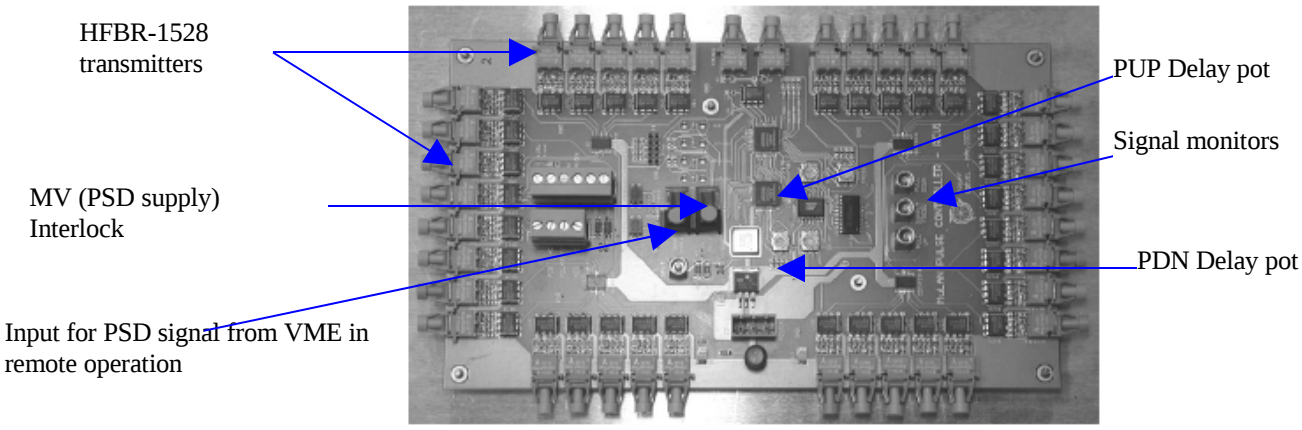

Figure 5. Mulan Pulse Controller Board (MPCB), courtesy of Michael Barnes.

Figure 6 illustrates the firing sequence of the RFQ drive signals. A justification for the PWM (Pulse Width Modulation) of these signals is provided Appendix A – 1kV board switching.

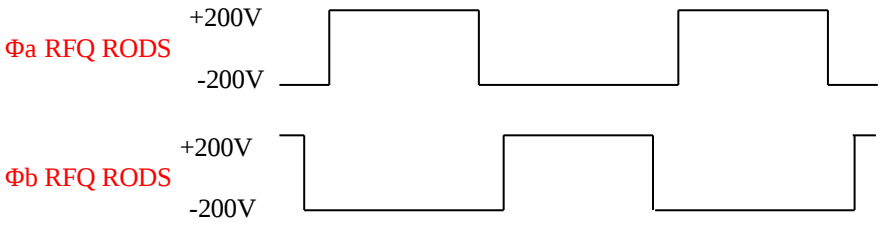

Figure 6. RFQ rods pulsing sequence: phase A (Φa) and phase B (Φb).

4.0 PHASE DRIVER RACKS

Each PDR (Figure 7) can house up to eight 1kV boards. The minimum distance between any two boards within the rack is approximately 5mm, which is sufficient to ensure that dielectric breakdown doesn't occur at RFQ voltages well above 400V. Presently there are six 1kV boards in each rack. The top three and bottom three cards constitute the "pull up" (PUP) and "pull down" (PDN) stacks respectively. The PUP and PDN stacks are driven by Φa and Φb respectively. Thus when the PUP (PDN) stack is turned on and the PDN (PUP) stack is off, the respective set of rods is charged (discharged) to a magnitude equal to half the supply voltage of positive (negative) polarity.

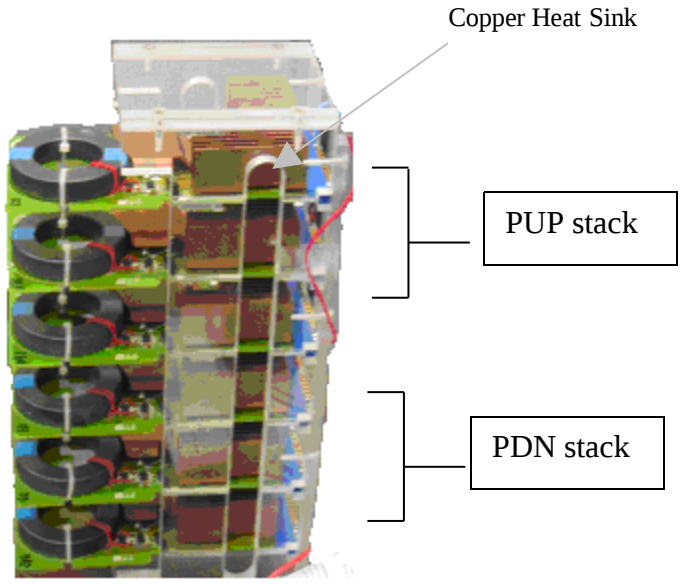

Figure 7. The Phase Driver Rack houses the 1kV boards used to drive the RFQ rods

A Xantrex XFR600-2 supply (600V @ 2A rating) provides the energy necessary to charge the total capacitive load consisting of the RFQ structure, the off-state stack, and parasitic capacitances to ground of the stack turning on. Unlike Capacitor Charged power supplies, the XFR600-2 isn't designed to deal with fast switching, high voltage pulses. An RF choke and a capacitive filter bank have been installed to prevent local oscillations from feeding back into the supply. The capacitor bank consists of five parallel high quality (low inductance and low ESR) Panasonic capacitors totaling 280nF. Upon startup this capacitive bank is charged up to the supply voltage and provides instant current required to charge the RFQ. The supply therefore "sees" a fairly constant DC voltage at its output terminals and provides a modest DC current to top-up the capacitive bank.

The charging pulse current flows from the capacitive bank through a series connected pair of current limiting resistors (90W MAX at 40˚C per resistor) totaling 75Ω, through the D-S chain of the PDR stack that is turning on (PUP stack), and finally onto the RFQ rods. Discharge pulse current flows from the rods through a similar pair of inline resistors to the ground side of the capacitor bank. Figure 8 shows the RFQ rod sets being charged and discharged to +200V and –200V respectively. The 75Ω power resistors are currently on order and different resistors are temporarily being used to drive the RFQ thus explaining the difference between fall and rise times.

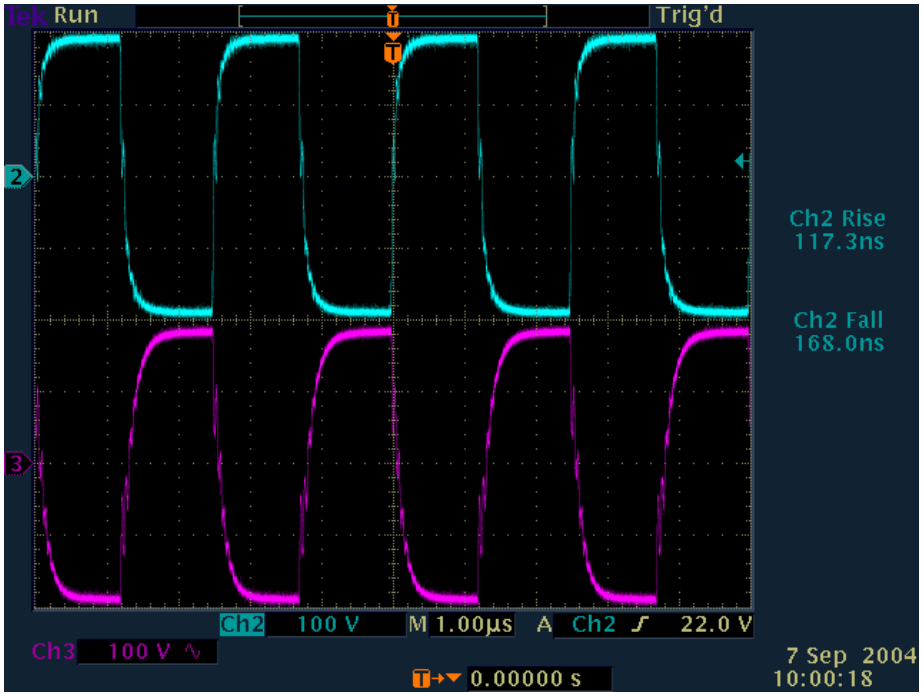

Figure 8. RFQ rods being driven at ±200 Volts. Signals are equal in magnitude and out of phase.

The power MOSFET on the 1kV boards (section 5.0) is rated at 72A pulsed. For operation at 400V peak to peak, a resistance of 5.6Ω is required to limit the current to a maximum of 72A. Since power dissipation is directly proportional to the square of the current and linearly proportional to resistance, the value of the current limiting resistance may be chosen at a higher value in order to reduce power consumption while still satisfying the required rise/fall times of 125nsec or less. It is vital to keep a sufficiently high ratio between the current limiting resistor and the MOSFET's on-state resistance in order to reduce lifetime degradation of the MOSFET by maintaining its junction at a sufficiently low temperature.

4.1 EFFECTIVE CAPACITANCE OF PDRs

As mentioned previously, each PDR consists of a PUP and a PDN stack. Proceeding the turn off of one stack the other stack is turned on. The stack that turns on carries the current which must charge the:

1. Output load (RFQ rods).
2. Off-state stack.
3. Parasitic capacitances to ground of the stack turning on.

4.1.1 Output load (RFQ Rods)

The RFQ is made up of four segmented rods that are 0.7 meters long (Figure 9). Each rod consists of 24 stainless steel electrodes that are physically isolated from one another by an air gap, and are mounted on a ceramic insulator that sits within a stainless steel yoke structure. Figure 9 shows the RFQ after its yoke structure had been modified due to forecasted electrical driving problems with the original yoke structure (Appendix D – RFQ YOKE). The four rods are mounted onto three square stainless steel support frames and the whole structure is mounted to the RFQ lid that is referenced to HV ground (Figures 9-10). The segmented rod structure allows for the application of an electrostatic field so as to confine the ions in the third dimension.

Simulations done by Michael Barnes using **Coulomb** (Integrated Engineering Software) indicate a capacitive load of approximately 230pF presented by the RFQ rods in Figure 9. Measurements were in agreement with simulation results (Appendix A – RFQ CAPACITANCE).

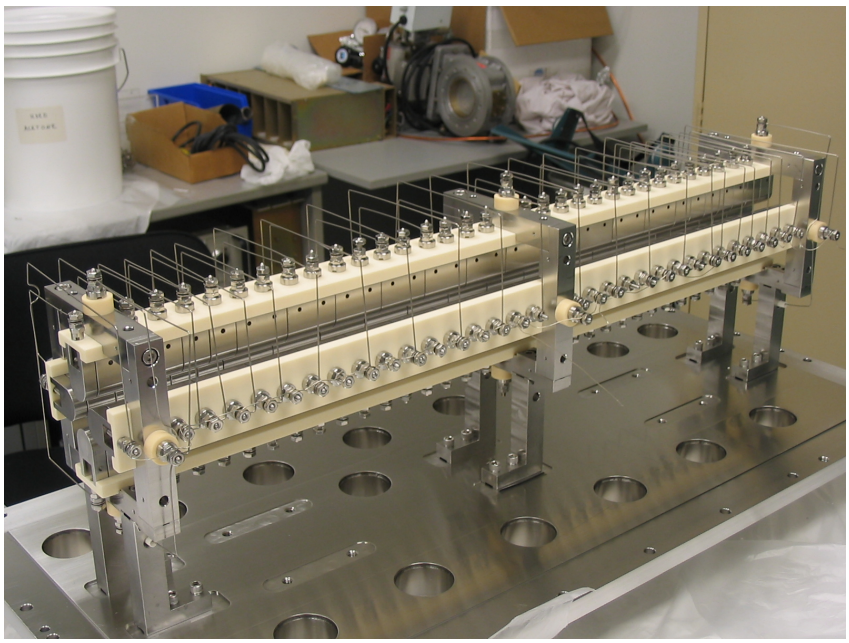

Figure 9. New RFQ yoke structure consists of 3 square support frames made of stainless steel.

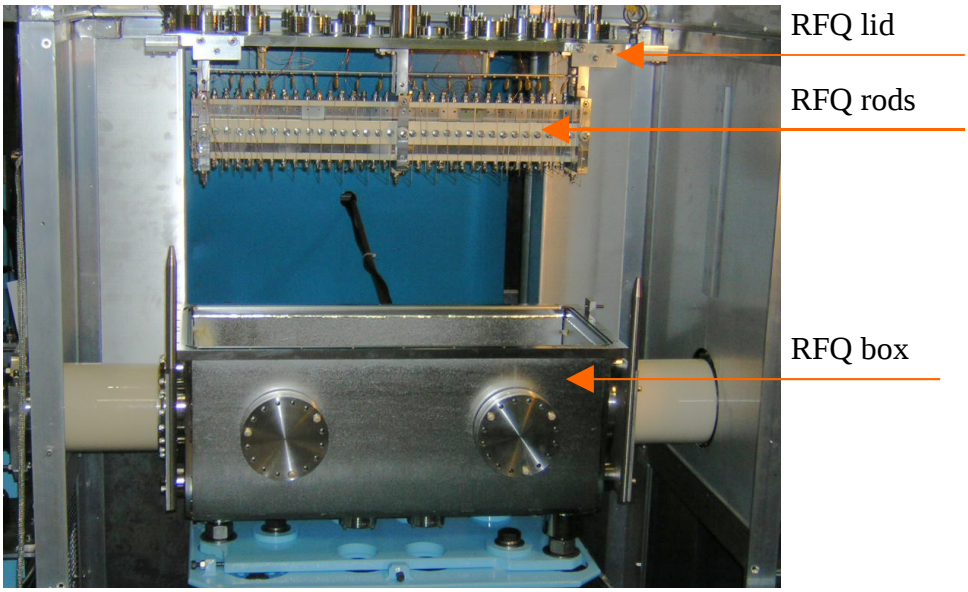

Figure 10. The RFQ is mounted to the underside of the lid and sits inside the RFQ box.

4.1.2 Off-state Stack

A DE375-102N12A MOSFET has a voltage dependent incremental capacitance between its drain (D) and source (S) terminals. The application of a D-S voltage across a MOSFET's output terminals leads to channel modulation. Channel modulation implies a modification in the geometry of the depletion region hence a change in the device's D-S capacitance value. Figure 11 shows the voltage dependent incremental capacitance and linearized effective capacitance of the DE375-102N12A [5]. Once the incremental capacitance is measured, the effective capacitance (= $2*E/V^2$) is derived from the amount of energy (E) that is required to charge the MOSFET's capacitance to voltage V [5].

With the current configuration of three 1kV boards per stack and a supply voltage of 400V, the effective capacitance of a DE-375-102N12A MOSFET is approximately 375pF. Three series connected boards per stack present a load of 125pF from the Drain of the top board to the Source of the bottom board.

4.1.3 Stack Turning On

DC grading resistors (Figure 12) ensure a good DC voltage grading in an off state stack. Ergo, prior to turn-on of a stack, the DC voltage is assumed to be graded linearly. Upon turn on of the stack, the parasitic capacitance to ground of 1.7pF [5] must be charged to the full DC voltage. Hence the 1kV board at the pulse end of the stack swings through the full voltage whereas the voltage through which the i^{th} 1kV board swings through is equal to (i/3) of the full DC voltage. For the PUP stack the source of the 1kV board that is at the pulse end of the stack is on the pulse deck whereas for the PDN stack it is the drain of the 1kV board at the pulse end of the stack that is on the pulse deck. Hence the parasitic capacitance to ground depends on whether the PUP or PDN stack is being considered. The parasitic capacitance to ground for the PUP and PDN stacks are given by **(1)** and **(2)** respectively [5].

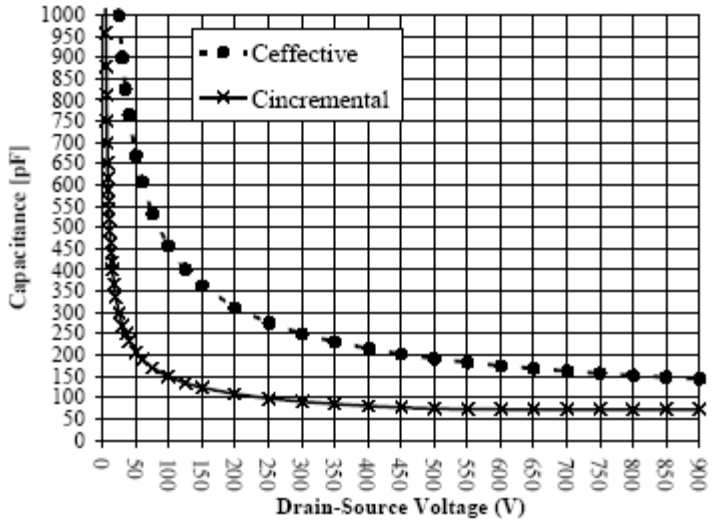

Figure 11. Measured voltage dependent incremental capacitance ($C_{incremental}$) and effective capacitance ($C_{effective}$) of a DE375-102N12A MOSFET. Courtesy of Michael Barnes.

$$\mathbf{Ceq\text{-}gndUp = \Sigma\ (i / 3)^2 * Cgnd(i)} \qquad \mathbf{(1)}$$

$$\mathbf{Ceq\text{-}gndDN = \Sigma\ ((i-1) / 3)^2 * Cgnd(i)} \qquad \mathbf{(2)}$$

where; Cgnd(i) is the capacitance to ground of the i^{th} 1kV board.

Capacitances to ground of the PUP and PDN stacks when they are turning on have not been measured. However, they will be insignificant relative to the capacitance contributed by the off-state stack and the RFQ.

The total capacitive load that is to be driven is therefore approximately composed of the RFQ capacitance and the off-state stack capacitance. Once the RFQ was placed in its box the average DC current of the Xantrex600-2 increased dramatically. The drive current at 400V ranged from 0.31A at 400kHz to 0.67A at 1MHz. An additional capacitance can be attributed to the HV connectors through which the RF signals are coupled onto the RFQ rods.

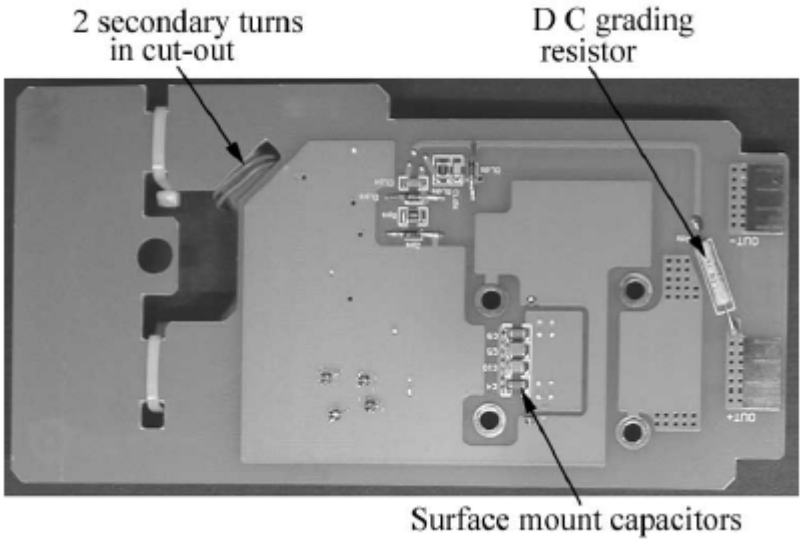

Figure 12. Underside of a 1kV board (Courtesy of Michael Barnes)

5.0 1kV BOARD

The function of a 1kV board is to act as an electronic switch that can rapidly transfer a significant amount of energy from the source to the load. The switch turns off whenever there is a sufficient amount of red light (650nm wavelength) present at the onboard fiber optic receiver 's input otherwise it is on.

The main components housed by a 1kV board are: one ferrite core, one fiber optic HFBR-2528 receiver, one DEIC420A MOSFET driver IC, and one DE375-102N12A RF power MOSFET (Figure 14). A single turn primary winding runs through the middle of the ferrite core. The PSD (section 6.0) sends current pulses through this primary winding. The pulse through the primary winding results in a changing magnetic field inside and around the core. This changing magnetic field induces a potential difference (voltage) across the secondary winding in accordance with Faraday's Law. The secondary winding is connected to a full-wave rectifier, consisting of 4 fast high-current ES1B diodes, whose output charges approximately 4 µF of surface mount capacitors which provide the onboard DC power. The onboard DC voltage is measured across capacitor C13.

Why use ferrite cores to provide the 1kV boards with a DC voltage instead of a DC supply?

The 1kV boards are driving a capacitive load. This implies that the source potential of the 1kV boards is not fixed but rather varies with respect to ground potential. Do to the inherent behaviour of an inductor, the ferrite core is able to track the changing source potential and still transfer the energy required to maintain proper onboard voltage, whereas a DC supply doesn't have this capability. Michael Barnes generated an electrical model of the ferrite core; the core has a magnetizing inductance of 9uH with a parallel resistance of 30Ω accounting for core losses. Simulations showed that at a PSD frequency of 350 kHz, corresponding to an RFQ frequency of 1.2 MHz, core losses of 6.5 µJ per pulse (2.5W) are expected. Another favourable

characteristic of this core (Amidon type F ferrite) is that it provides a linear relationship between the frequency of the primary pulse and the secondary load current.

The +5V supply voltage for the HFBR-2528 receiver is derived from the onboard 16V via a 220 Ω resistor, Rfo, and a 5V zener diode, Zfo [5]. The upper frequency limit of operation of a 1kV board is imposed by the HFBR-2528 fiber optic receiver rated for a maximum of 10 MBaud, otherwise the basic design of the board is limited by power dissipation and has been tested successfully up to frequencies of 3.5 MHz [5].

The value of C_{11} is based on the propagation delay of the turn on command measured from the TTL input to the output pulse. The TTL input is taken from the PUP input on the MPCB (section 3.0) and the output is measured between the drain and source terminals of the 1kV board. Since a logic low input results in the power MOSFET turning on, the delay is measured from the 0.8V mark (maximum value for TTL low) on the falling edge of the TTL signal to the point where the output starts to swing low (negative edge). Initially, the delays of all the boards are measured with no C11 in place (Appendix A – Table 1). A reference delay that is slightly larger than the largest measured delay is chosen as the propagation delay value to which all the boards are trimmed. A reference delay of 160µsec was chosen for this system.

The circuit looking into the MOSFET driver (pin 2) from the output of the receiver (pin1) is shown in Figure 13. This is a first order RC integrator and the voltage at the input of the MOSFET driver is governed by equation **(3)**. The driver typically switches between 3 - 3.5V (60% – 70 % of receiver supply voltage). Therefore, once the receiver output goes high, it takes about one time constant (τ) before the driver is switched. Equation **(4)** was derived empirically and is used to calculate the value of C_{11} required to increase the delay to 160µsec. Note that it is imperative that the receiver solder connections be carefully checked in order to ensure that its supply voltage is close to 5V, otherwise the driver turn-on delay will be higher than calculated or worse yet, the card may not switch do to a low signal voltage at the MOSFET driver's input. The fiber optic receiver typically turns on somewhere between 3-3.5 Volts which is between 60-70% of the receiver's supply voltage. This implies that it should take approximately one time constant, τ, to charge up the relevant capacitance in addition to the driver's inherent delay, before the output switches. Ensuring that the MOSFET driver's supply voltage is fairly consistent throughout the boards is critical since its inherent delay is voltage dependent and plays a part in the total propagation delay.

$$\mathbf{Vc(t) = Vin * e^{-t/\tau} + V_0} \qquad \mathbf{(3)}$$

where; $\mathbf{\tau = R_2 * C_{11}}$,
$\mathbf{V_0 = Vc(0)}$, **Vin = Receiver voltage at pin 1.**

$$\mathbf{C_{11} = 0.9 / (R_2 * t_{delay})\ Farads} \qquad \mathbf{(4)}$$

where; $\mathbf{t_{delay}}$ **= 160µsec – delay without C11,**
$\mathbf{R_2 = 681\Omega}$.

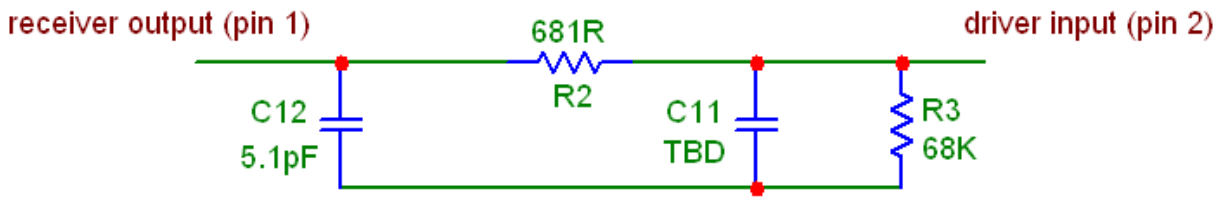

Figure 13. First order charging circuit between receiver output and MOSFET driver input.

The current drawn from the 4uF of onboard capacitance is composed of I_1 and I_2. I_1, equation **(5),** is fixed at 50mA while I_2, equation **(6)**, is linearly dependent on the frequency at which the receiver is being triggered at and is mainly used to charge the 11nF of capacitance, composed of the MOSFET driver's output and power MOSFET's input capacitances, from 0V to Vcc. I_2 varies from 70mA to 176mA for a frequency range of 400kHz to 1.2MHz.

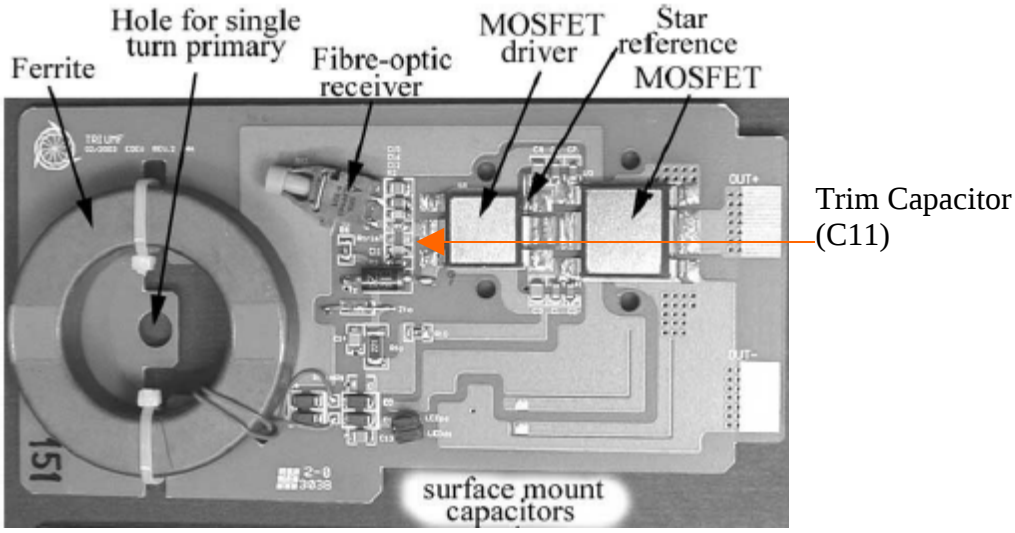

Figure 14. Top side of 1kV board (receiver shield and heat sink removed to show components underneath). Courtesy of Michael Barnes.

$$\mathbf{I_1 = (Vdc - Vzfo)/Rfo} \qquad \mathbf{(5)}$$

$$\mathbf{I_2 = C*\Delta V*f_{rfq}} \qquad \mathbf{(6)}$$

where; **Vdc is the onboard DC voltage,**
ΔV = Vcc,
f_{rfq} = receiver trigger frequency,
C = 11nF.

In total, the 1kV board draws 120mA to 226mA at operation spanning from 400 kHz to 1.2 MHz. Resistor R_{10} serves as a probe resistor and to protect the MOSFET driver by providing some control over the current path taken by transients on the supply lines. The average current through and power dissipated by R10 are given by equations (7) and (8) respectively. At 1MHz R10 will dissipate 37mW. Future operation at 3.0 MHz requires that R10 be upgraded to a 1W resistor. R10 will be dissipating one third of its power rating at the latter frequency and life time degradation do to heat dissipation will be minimized.

$$\mathbf{I_{avg} = 176nC * f_{rfq}} \qquad \mathbf{(7)}$$

$$\mathbf{P_{R10} = i^2 * R_{10}} \qquad \mathbf{(8)}$$

where; $\mathbf{f_{rfq}}$ **= receiver trigger frequency,**
$\mathbf{R_{10} = 1.2\Omega}$

A star reference point for the 16V DC power supply, and fiber optic receiver is taken from the top of one of the MOSFET driver's output legs (Figure 14). This reference point is chosen as it minimizes the effect of transients, resulting from a large rate of change of output current of the MOSFET driver, upon the receiver [5]. Each 1kV board has a DC grading resistor, Rds, with a nominal value of 1.6MΩ, and red and yellow LEDs that provide diagnostics for the D-S voltage and the 16V DC power supply respectively. When a high voltage is present across D-S of the RF power MOSFET the red LED turns on. An 18V tranzorb (Tz) limits the low voltage DC power supply to a safe level for the components.

The power MOSFET is sandwiched between the PCB and a copper heat sink to provide double sided cooling. The copper heat sink (Figure 7) has fins to provide additional surface area for improved cooling. The copper plate's total surface area is ~165 cm^2. A heat sink temperature of 40ºC has been chosen in order to ensure that the MOSFET's temperature is at a reasonable operating point. Appendix C contains curves pertaining to calorific measurements made in ambient air temperature of 20.3 °C at various airflows. These curves are used to determine MOSFET power dissipation vs. heat sink temperature for a given air flow.

6.0 PSD

The PSD provides the primary current pulse necessary to energize the 1kV boards. This energy is mainly used to power the fiber optic receiver and MOSFET driver. The layout of the board (Appendix A) is similar to the 1kV board with some exceptions. Rather than employing a ferrite core, a floating 12V supply is used to power the board. Rfo is chosen to be 150Ω instead of 220Ω to ensure that there is sufficient current to operate the zener diode, Zfo, and receiver, RX1. Presently, R10 is a 1.2Ω, ¼ W resistor. The ¼ W power rating is sufficient for the current PSD frequency range. If the RFQ is to be triggered at frequencies beyond 2 MHz, R10's power rating should be increased to ½ W in order to compensate for the extra power dissipation. Equations (7) and (8) give the average current through and power dissipated by R10 respectively with the substitution of the PSD driving frequency, f_{psd}, with f_{rfq}. For RFQ operation at 1MHz the

corresponding PSD frequency is 278kHz giving an average current of 49mA through R_{10} and a power dissipation of 29mW.

The PSD board has an extra transmitter (TXds) acting as an interlock that feeds into the MPCB. This interlock ensures that the PSD's onboard receiver, RX1, isn't trigged until the current pulse supply (XFR300-4) voltage reached 160V. Otherwise, the possibility of a latch-up condition leading to local oscillations between the power MOSFET (U2) and MOSFET driver (U1) would result in overloading of the 12V supply and consequently in PSD malfunction. Once the supply voltage has reached approximately 160V, TXds turns on and the transmitters driving the 1kV board(s) in the PDRs and PSD are enabled.

Pads 3 and 4 are connected to the terminals of a Xantrex XFR300-4 (300V at 4A max rating) power supply via line filters (Appendix A). The supply charges CfilA1, CfilA2, and Cfilb while the power MOSFET is turned off. These capacitors provide the charge for the current pulse (Figure 15) upon turn-on of the power MOSFET (U2). The current exits at PAD 1, flows through a 63 ohm series resistor, through the primary turn of the twelve ferrite cores, and returns via PAD 2. An additional RC (Cgrad and Rgrad) current path is connected from the drain to the source of U2. This RC branch acts as an alternate current path in an effort to attenuate voltage transients present upon turn-off of U2. Following turn-off of U2, an inductive primary current with a peak amplitude of 2.2A continues to flow for the duration of the current pulse fall time. The exclusion of the latter current path would cause the drain voltage of the power MOSFET to climb to high levels possibly leading to avalanche breakdown and damaging the solid-state device.

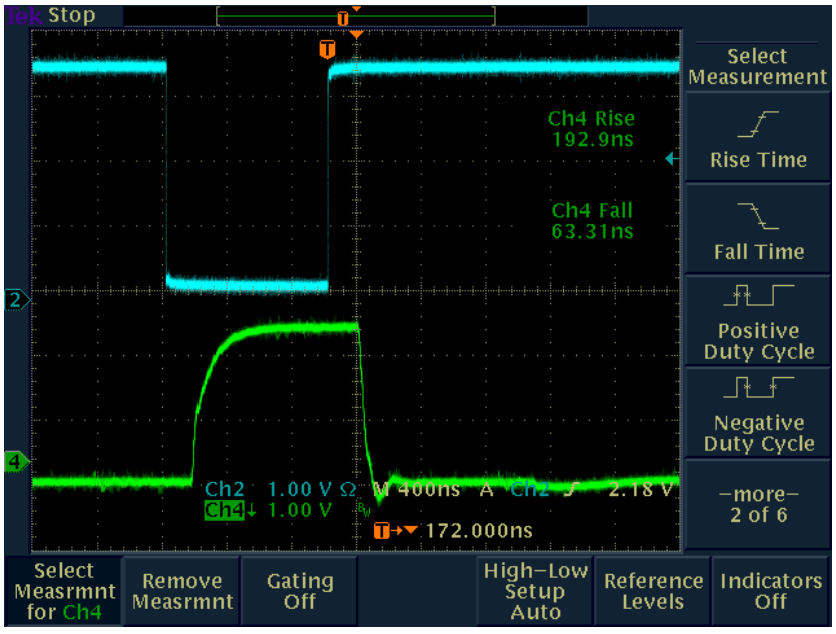

Figure 15. Inverted PSD (1µsec pulse width) drive signal (top). PSD (1µsec pulse width) output current pulse (bottom)

The PSD trigger frequency depends on the secondary current drawn by the 1kV boards, which is in turn dictated by the rate at which the 1kV boards are being triggered (Appendix B – Table 1). The resistance in series with the ferrite cores is directly proportional to the number of 1kV boards being energized. For every 1kV Board five to six ohms of resistance is added (60Ω - 72Ω for six boards). This is done in order to ensure that the R/L time constant remains fixed. Too high a resistance value will lead to too large a time constant and a reduction in the onboard DC voltage of the 1kV boards. This may result in oscillatory feedback between the receiver and MOSFET driver resulting in system malfunction. If the current limiting resistance is too small, unnecessary thermal stresses will be imposed on the solid-state components and power consumption will increase needlessly.

Recent upgrades for the PSD are as follows:

- Replacement of surface mount inductors L1 and L2 with short circuits.
- Addition of three filter boards designed by Michael Barnes (Appendix A). These filters attenuate any transients feeding back into the 12V and 300V supplies and minimize RF radiation. The boards were etched by Dyco Circuits Inc. http://www.dyco-circuits.com/ and populated in the TITAN lab. Box designs were done using AutoCAD (Appendix D) and modifications were done in-house by the Machine Shop.
- Addition of RC (2R2, 150nF) networks from Mvin+ and Mvin- lines to ground.
- Addition of 150nF capacitor between Mvin+ and Mvin-.

Further PSD upgrades to be done:

- Addition of two parallel 10R, 3W resistors inline from Mvin+ to the +300V BNC lead.
- Replacement of Rfilc and Rfild with short circuits.
- Replacement of Rfila and Rfilb with 47R resistors.

Extra PSD boxes have been made for future system upgrades and ongoing lab testing. Box modification drawings were produced with AutoCAD (Appendix D) and the job was submitted in-house to the Machine Shop.

7.0 EXTRACTION PULSE

The ion beam enters the RFQ from one end and is cooled and trapped via collisions with an inert gas and the application of an RF quadrupole field configuration. The trapped ion bunches must be extracted from the opposite end of the RFQ and sent into the EBIT at a rate of 8-20 Hz. The potential gradient used to accomplish this is shown in Figure 16. This potential gradient is achieved by adding a positive and negative DC offset to the 22nd and 24th electrodes, respectively, of every pole. The extraction pulse DC offset is applied for a duration of 50-100μsec and returns to the trapping DC potential for the remainder of the pulse. The summing scheme of the RF and

extraction pulse signals is shown in Figure 17. The resistance in series with the McGill pulser is chosen such that the rise time of the extraction pulse is below 10μs. Simulations with Micro-Cap show a 20 to 30 percent droop in the RF signal's magnitude at the 22nd and 24th electrodes. This is do to the aforementioned rise time restriction. This droop, however, is acceptable since the phenomenon is present on all four rods and the quadrupole hyperbolic field configuration should be preserved

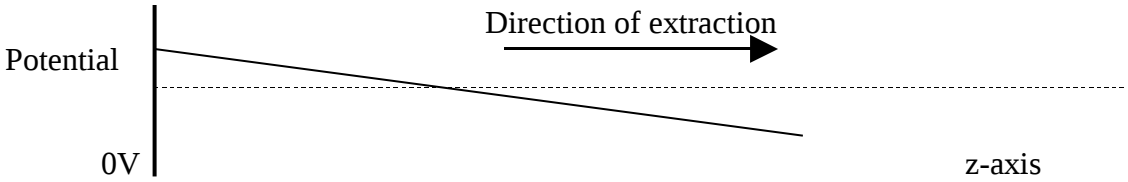

Figure 16. Extraction pulse potential gradient vs. horizontal displacement from 22nd to 24th electrode.

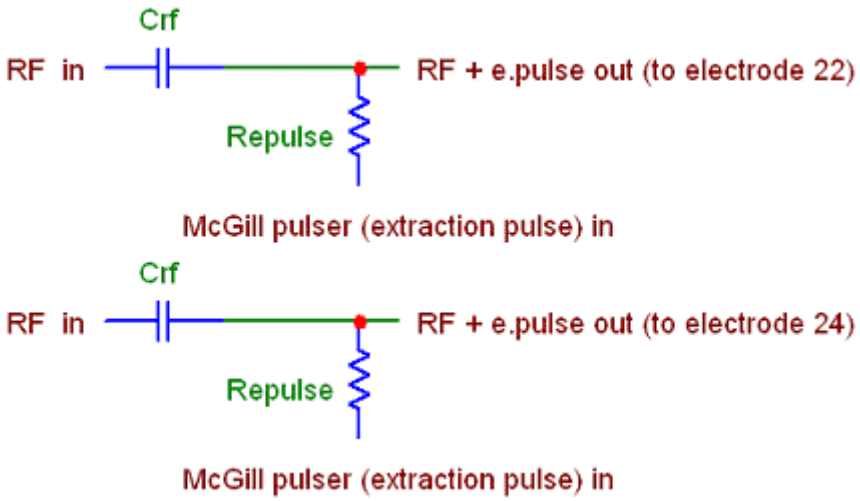

Figure 17. RF and extraction pulse superposition scheme on electrodes 22 and 24.

Figure 18 shows the circuit used to model the extraction stage and the superposition of the RF and extraction pulse waveforms on electrodes 22 and 24. Figure 19 shows the decoupled RF and extraction pulse waveforms on electrodes 22 and 24.

Note: The extraction pulse has a positive pulse width of 100usec. Here it is shown with a fifty percent duty cycle for illustration purpose only.

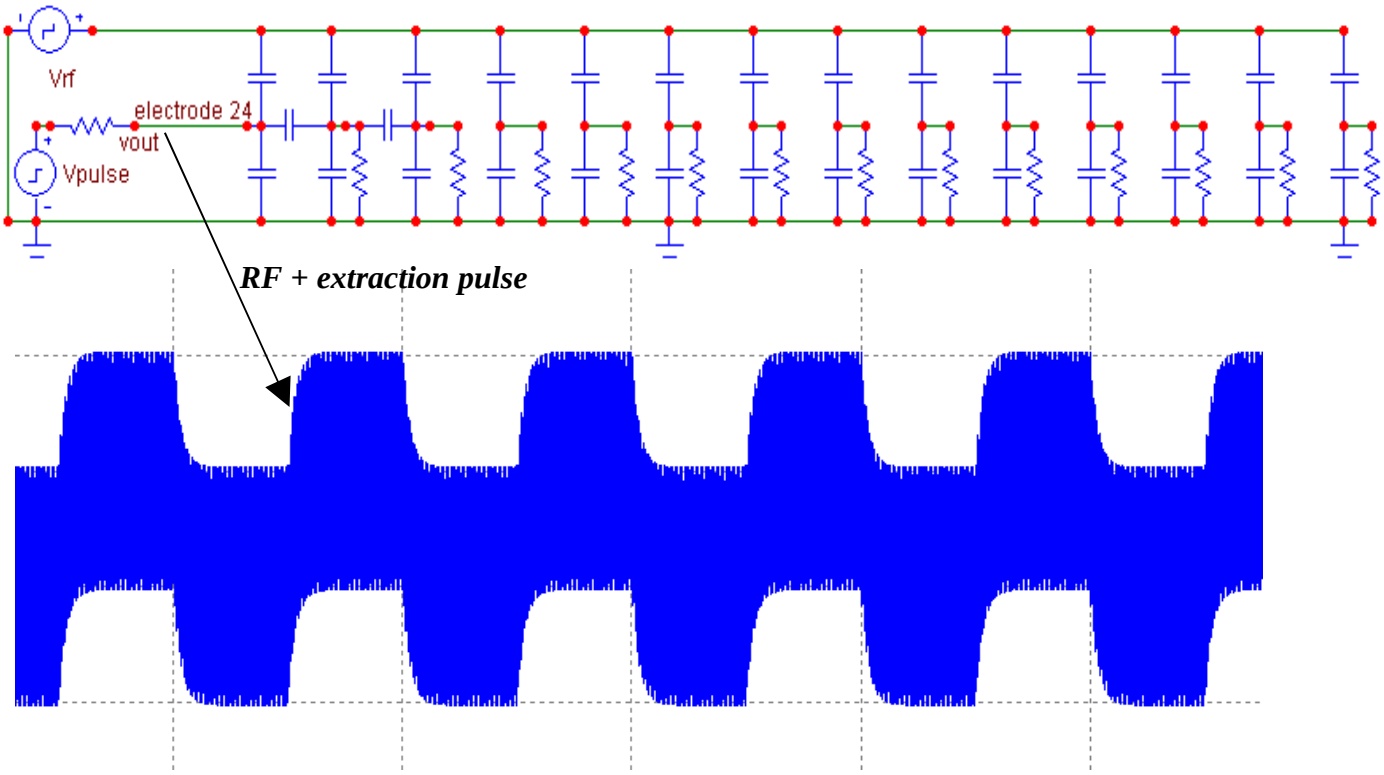

Figure 18. Circuit model of extraction stage (top), and superimposed RF and extraction pulse signals (bottom).

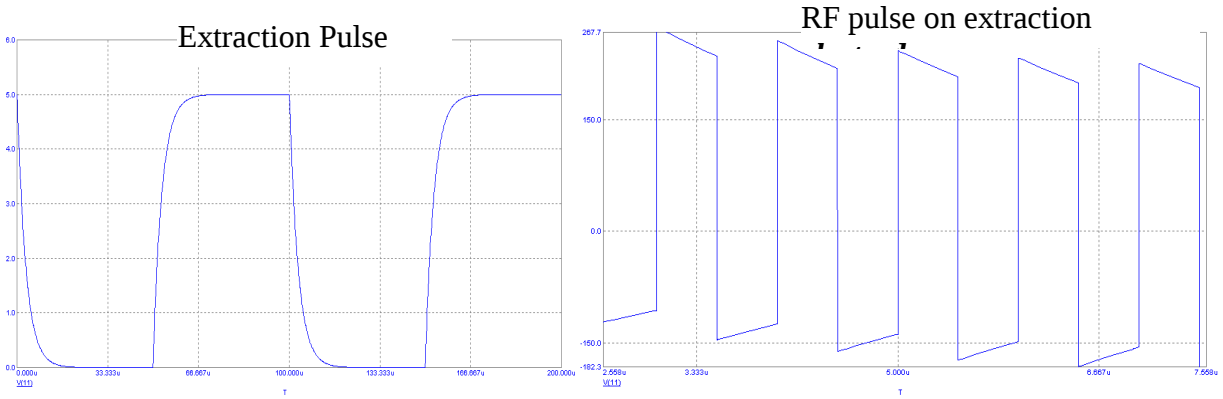

Figure 19. Decoupled RF and extraction pulse waveforms on electrodes 22 and 24.

8.0 INTERLOCK BOARD

The Interlock Board has safety interlocks for the MV power supply (XFR300-4), all of the cooling fans, and spare interlocks for expandability. The board has not been fabricated yet, but with the exception of modifications mentioned below, its design is complete. The layout will be similar to the **Slave PSI Kicker Interlock Board** (Appendix E). The purpose for having the MV power supply interlock is provided in section 6.0. The fan interlock detects a condition whereby the fan is not operating at its full capacity (full speed operation) and causes the system to shut down in order to prevent overheating of the 1kV board components. In the current design, the fan interlock monitors the current flowing through the fan motor and trips if the current goes below a minimum threshold. Another fault condition that should be detected is a stalled fan. If a fan stalls, the current flowing through its motor, impeded only by the DC coil resistance, will be larger than the current under full speed operation. Until recently, it was assumed that the fan's thermal impedance overload protection would respond quickly enough under a fault condition and prevent damage to the 1kV boards. Lab tests have nullified that assumption for the worst-case condition of a stalled fan. Hence, the Interlock Board will be modified to account for this fault condition, the modification consisting of the inclusion of an upper threshold for the fan current. Once the fan current exceeds the upper threshold the fan interlock will trip and cause the system to shut down in order for the fault to be remedied.

Note: Under a stall condition the thermal impedance overload protection is slow to react because the internal coil temperature must reach approximately 140˚C prior to its actuation. Data sheets provide thermal protection reaction time once the coil has reached a specific temperature (typically 130-140 ˚C), the reaction time being on the order of milliseconds. The data sheets do not, however, mention how long the pertinent coil section takes to reach that temperature under various fault conditions.

8.1 INTERLOCK BOARD OPERATION

This section describes the full operation of the Interlock Board (refer to Appendix D for complete schematic).

8.1.1 Fan Interlock Operation

The LM311 op-amp functions as a two input comparator. The signal feeding the positive input is the lower threshold and an equivalent DC voltage corresponding to the AC fan current feeds the negative input. The AC fan current is fed to the primary of a transformer. This current induces a voltage on the secondary, which is then rectified and filtered to produce a DC voltage. P1 (10kΩ potentiometer) is used to adjust the lower threshold as required. The output of the comparator is fed to the negative supply rail of a SPDT (Single Pole Double Throw) relay (K1). Under a fault condition whereby insufficient current is flowing through the fan, the lower threshold value will exceed the DC equivalent fan voltage and the op-amp's output will approach the value of the positive rail (15V in this case). Under such a condition the relay is de-energized and the closed set of contacts will be as shown in Figure 20. As a consequence LED1 will now turn on and pin 3 of K1 will loose its ground connection. Pin 3 of K1 is connected to pin 4 of the subsequent relay, K2, which is fed by the comparator output pertaining to FAN 2. Relays K1 – K6 are daisy chained in such manner. Pin 3 of K6 is the FAN-INTLK-SUM pin. Under normal

operating conditions there is a closed contact between pins 3 and 4 of every relay. Pin 4 of relay K1 is referenced to ground and as a result, so is the FAN-INTLK-SUM pin. If any fan fails the connection to ground will be lost and the FAN-INTLK-SUM pin will be referenced to pin 2- an open contact.

The FAN-INTLK-SUM pin is connected to the negative supply rail of relay K9. The relay is energized or de-energized when the FAN-INTLK-SUM pin is referenced to ground or an open contact respectively. J1 under "LOCAL INTERLOCK SUMMARY CONTACTS" provides an electrical indication of a fan fault condition. Under normal operation FAN-INTLK-COM and FAN-INTLK-NO pins are shorted together (pins 3 and 4 of K9) and referenced to ground whereas under a fault condition they are floating open contacts. Under a fault condition the FAN-TRIP pin (pin 9 of K9) will be connected to ground. This signal is connected to pin 3 of J13 ("TO LED DISPLAY BOARD") and an LED turns on to indicate that a fan has tripped. Thus there are two visual and one electrical indicator(s).

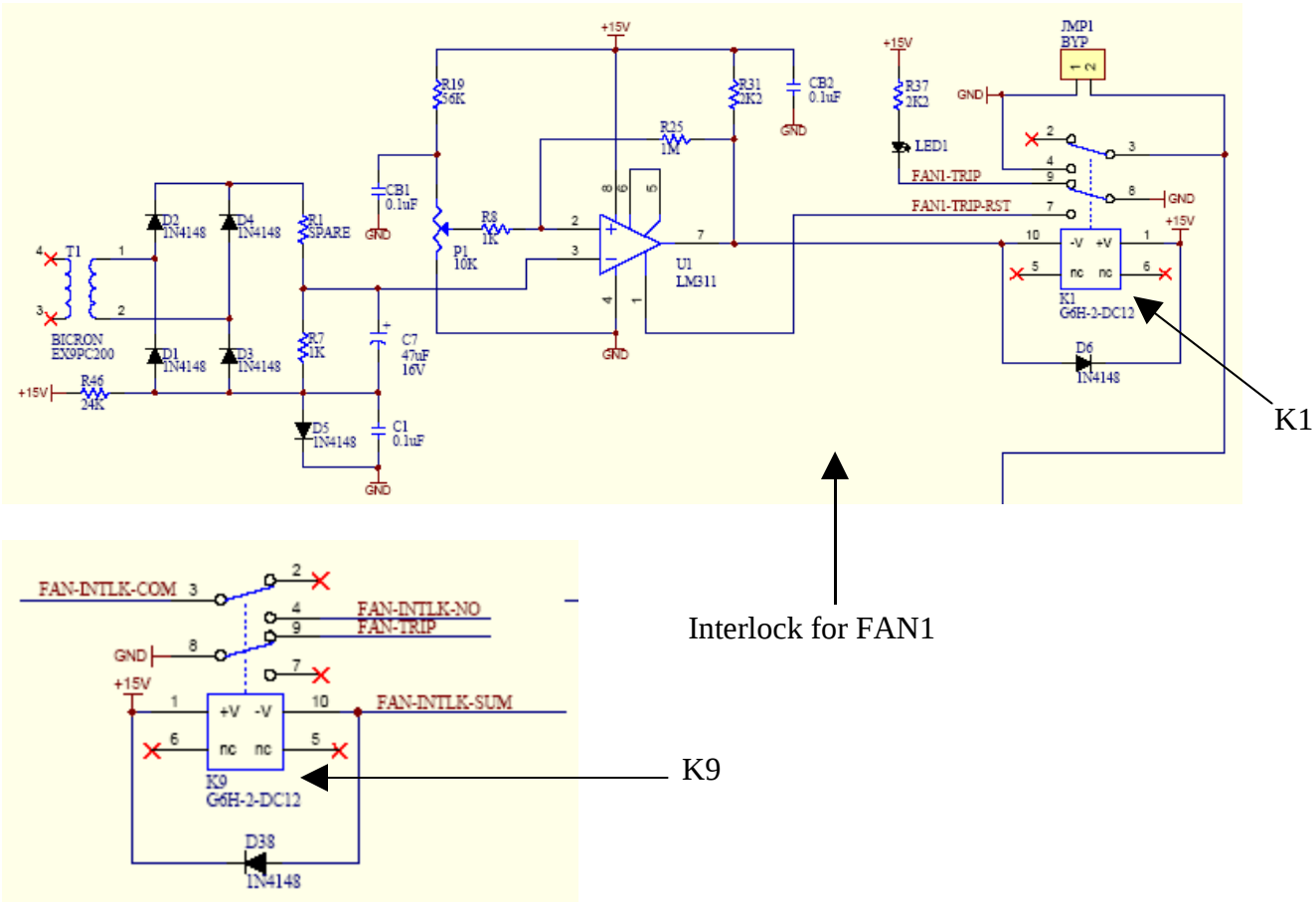

Figure 20. FAN interlock scheme on PSI Kicker Interlock Board.

8.1.2 MV power supply Interlock Operation

Once RX1 receives a signal from TX1 (see section PSD), pin10 of K11 (Figure 21) is at ground potential and the relay is energized. Under this condition pins 1 and 2 of J13 under "LOCAL INTERLOCK SUMMARY CONTACTS" are shorted together at ground potential. Otherwise, the two contacts are floating open connections. Pin 1 of J13 under "TO LED DISPLAY BOARD" is connected to the MV-PS-OK pin of K11 and causes an LED to turn on under a no-fault condition. Thus there is one visual and one electrical fault indicator.

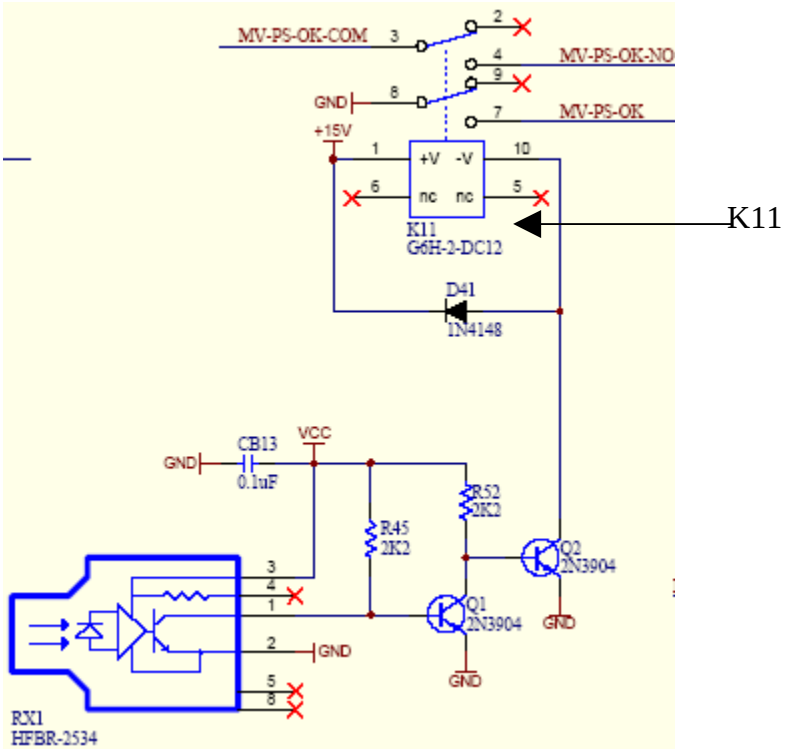

Figure 21. MV power supply interlock scheme on PSI Kicker Interlock Board.

CONCLUSION

The test data confirms that the HVRF Square Wave Generator for TITAN's RFQ Ion Trap is capable of driving the RFQ rod structure beyond the required specifications. The specifications call for a square wave at frequencies spanning 0.4-1.0 MHz with a peak-to-peak magnitude of 400V and rise and fall times equal to or less than 125nsec. The current system has been tested at the aforementioned frequencies and amplitude with rise and fall times below 125nsec.

RECOMMENDATIONS

Recommendations with regards to the further development of the HVRF Square Wave Generator for TITAN's RFQ Ion Trap are as follows:

1) Make calorific measurements to determine the variation in power MOSFET heat sink temperatures with the current fan arrangement.
2) If there are significant variations in heat sink temperatures consider the implementation of a cross flow AC blower for achieving laminar air flow thus reducing temperature variations. If RF noise becomes an issue the use of RF shielding honeycomb (contact: karen@aierep.com) may resolve both RF and air flow issues in which case the current Tarzan fans can be used.
3) Monitor the supply lines of the various power supplies in use to see what level of power line oscillations they are exposed to and thus determine if further filtering is required.
4) The propagation delay of the DEIC420 MOSFET driver is dependent upon the magnitude of its supply voltage. This plays a role in the total propagation delay pertaining to a 1kV board. If necessary, MOSFET driver delays can be matched to a higher degree by narrowing the range of onboard DC voltages on the 1kV boards (measured across C13). This may be done, by adjusting the value of C13 or experimenting with spare ferrite cores.
5) If the extraction pulse rise time is inadequate for shutting the trap, consider implementing a double trap scheme whereby the ions are collected in one trap and extracted from a second trap.
6) Modify the MPCB to accept a fiber optic RFQ drive signal rather than an electrical signal for better noise immunity.
7) Use the information and equations provided in sections 5.0 and 6.0 to determine component values required for system upgrades (increasing voltage and frequency). Use the spare slots in the PDRs to add additional cards for driving the RFQ at peak-to-peak voltages beyond 1kV. Note that the power consumed by the power resistors (ceramic tubes) should be calculated in order to determine if higher rated power resistors are required.
8) Always test any modifications on the test setup in the labs before modifying the HVRFSWG in the RFQ Driver Rack.

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