Implementation of the Electronics for a Radio Frequency Quadrupole

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Preface

The purpose of this report is both to fulfill part of the term requirements of The University of British Columbia's Co-op Engineering Program and to document the design, functionality, and operation of the electronics used in TITAN's RFQ ion beam cooler and buncher.

During my work term at TRIUMF within the TITAN group, I implemented, tested, and modified a high-voltage high-frequency digital switch used to drive the Radio-Frequency Quadrupole (RFQ), a key component in TITAN (TRIUMF's Ion Trap for Atomic and Nuclear Science). The main goal of TITAN is to gather high-accuracy mass measurements, with implied uses in the fields of nuclear, atomic, and solid-state physics. Obtaining ions from TRIUMF's Isotope Separation and Acceleration (ISAC) facility, the RFQ uses alternating electric fields and an inert buffer gas to slow down and focus the ion beam.

Summary

This report presents the implementation of the electronics for a radio-frequency quadrupole (RFQ) dedicated to TRIUMF's Ion Trap for Atomic and Nuclear Science. The RFQ requires a system that charges opposite pairs of electrodes to 500V above and below a 60kV reference at up to a frequency of 3MHz.

The electronics consist mainly of two 'stacks' of eight boards in series in a push-pull configuration. Each board contains an n-type enhancement power MOSFET and its support circuitry, most notably a MOSFET driver and a ferrite pulse transformer to provide 16V DC power. The boards are controlled remotely via a fiber-optic link from a pulse controller board. This board is situated 5m away from the stacks and within a faraday cage to reduce electromagnetic interference.

Both the 1kv stacks and the power supply driver that supplies power to the stacks are capable of generating strong electromagnetic fields, which can reduce the system's operational capabilities drastically. Therefore, a great deal of attention has to be paid to make sure that the various components of the RFQ electronics are as resistant as possible to the electromagnetic fields generated by itself. This means that wires should be kept as short as possible and preferably in twisted pair or coaxial cable.

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List of Abbreviations

EBIT:	Electron Beam Ion Trap
HVPS:	High Voltage Power Supply
ISAC:	Isotope Separator and Accelerator
MOSFET:	Metal-Oxide Semiconductor Field Effect Transistor
MVPS:	Medium Voltage Power Supply
RFQ:	Radio Frequency Quadrupole
PSD:	Power Supply Driver
TITAN:	TRIUMF's Ion Trap for Atomic and Nuclear Science
TRIUMF:	Tri-University Meson Facility
TTL:	Transistor-Transistor Logic

1.0 Introduction

This report presents the development of a high-voltage radio-frequency driver for the Radio Frequency Quadrupole (RFQ) cooler and buncher module of the TITAN facility, or Triumf's Ion Trap for Atomic and Nuclear science. The RFQ requires up to a 1kV 3MHz square wave to confine the smallest of ions of interest. Currently, the driver can output a square wave of $600V_{pp}$ and 2.2MHz to a test load.

1.1 TITAN

TITAN is a proposed second-generation facility for high-accuracy mass measurements of exotic isotopes. The facility consists of a RFQ Cooler/Buncher, an Electron Beam Ion Trap (EBIT) charge breeder, a Wien Filter, a Four-Way Switch, and a Penning Trap.

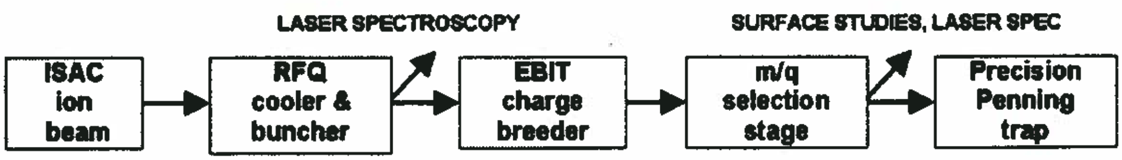


Figure 1. TITAN.

1.2 RFQ

The gas-filled RFQ will receive a continuous ion beam from ISAC (Isotope Separator and Accelerator), cooling and bunching it, before sending it to the Four-Way Switch. The ions will collide with the inert gas, thereby losing kinetic energy. By alternating the polarity on its four sets of electrodes, and hence the electric fields within, the RFQ can force the beam of ions towards its axis of symmetry. Meanwhile, the inert gas will be unaffected.

The stability of ions of a particular isotope varies with its mass, the magnitude of the electric fields, and the RFQ drive frequency. A formula to measure the stability of ions within the RFQ is defined as:

$$q = (2*e*V_{pp})/(m * r_o^2 * \Omega^2),$$

Where e is the ion charge, V_{pp} is the RFQ peak-to-peak voltage, m is the ion mass, r_o is the RFQ radius, and Ω is the RFQ angular frequency. The upper limit of q for stability is 0.908 for a conventional RFQ and 0.712 for a square-wave system such as this one. The system will be run at an operational point of q = 0.3 for optimal stability and acceptance. Analysis of the above equation shows that if the isotope mass is small, then, in order to maintain stability, either the RFQ frequency must be increased or the voltage has to be decreased. However, decreasing the drive voltage lowers the acceptance and, hence, the number of ions that can be injected into the RFQ. Increasing the frequency is more ideal for this reason and also because the ions would become focused faster.

This report covers all major components of the RFQ driver: the pulse controller board, the power supply driver, and the 1kV stack.

2.0 Pulse Controller Board

The pulse controller board can be considered the brain of the RFQ electronics system, controlling both the power supply driver and the stack of power MOSFET boards.

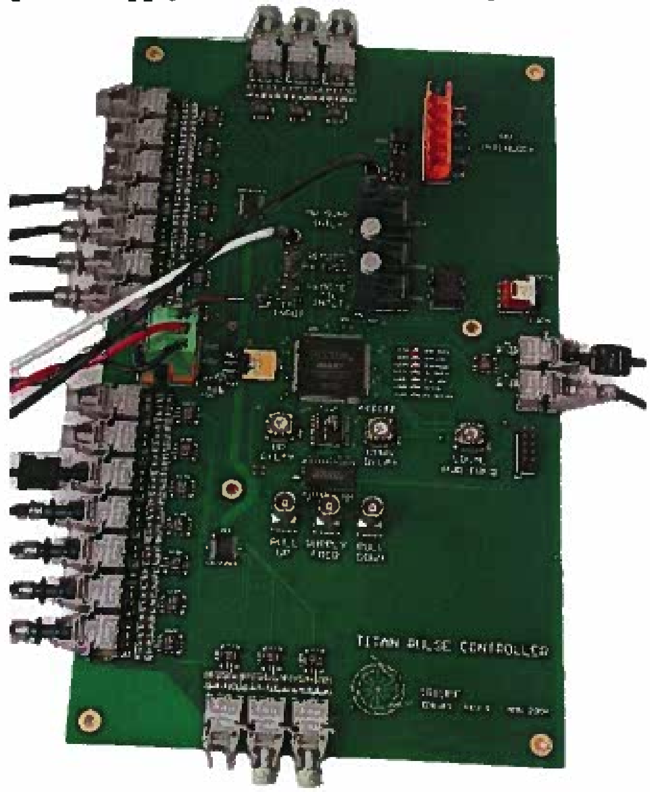


Figure 2. TITAN Pulse Controller Board.

2.1 Power Supply

Specifically designed for the TITAN project, this PCB contains an Altera FPGA and a variety of fiber-optic and TTL input and outputs along with their associated driver circuitry. A +5V power supply runs most of the components, with the exception of the FPGA that requires +3.3V provided by an onboard voltage regulator. Approximately 0.58A is drawn when the board is idle and 0.82A when the board is switching at 3MHz.

2.2 Operation

The controller board accepts an RFQ Frequency input from a signal generator via a LEMO connector cable in standard TTL logic. The Altera FPGA creates two signals from the input, a copy and an inverted copy. Both copies' duty cycles are decreased slightly to ensure that one signal is low before the other signal goes high. This delay is necessary to prevent the stack from shorting the power supply. It can be set between 11 and 56 nanoseconds by two onboard potentiometers. 10 HFBR-1528 transmitters for each copy convert the electric signals into optical signals that are then transmitted to the MOSFET stack using HFBR-RNS005 5m plastic fibre cable.

There is a third potentiometer that sets the power supply driver frequency between 166kHz and 333kHz. The output, two infrared transmitters, only activates when it senses a light from the Medium Voltage Interlock. This happens only when the Medium Voltage Power Supply's voltage is high enough that turning on the PSD power MOSFET would not cause it to latch. Usually, this condition occurs when the MOSFET's gate is driven high without a voltage difference being applied across the drain and source.

2.3 Noise Considerations

Originally, the controller board was situated approximately half a meter from the 1kV stack and PSD. Monitoring of the 5V power supply line on the oscilloscope with the stack driven at $300V_{pp}$ and 400kHz revealed a substantial amount of electromagnetic noise. At $400V_{pp}$ and 1.8MHz, the EM noise becomes so bad that the Altera board stops functioning. When this happens, the PSD and 1kV stack consequently stop switching and producing electromagnetic fields. Without electromagnetic interference, the Altera board then starts up again, resulting in a cyclic loop where the stack and PSD keeps activating and deactivating.

By using longer 5m fiber-optic cables and moving the pulse controller board farther away from the other components, the noise coupling can be greatly reduced. Wrapping the board with a layer of insulator to prevent conduction and a layer of aluminum foil acting as a Faraday cage also helps to attenuate the noise signal.

3.0 Power Supply Driver

The power supply driver is required to power the power MOSFET boards. As shown in the figure below, it is essentially another MOSFET board but with additional circuitry to buffer the current pulse.

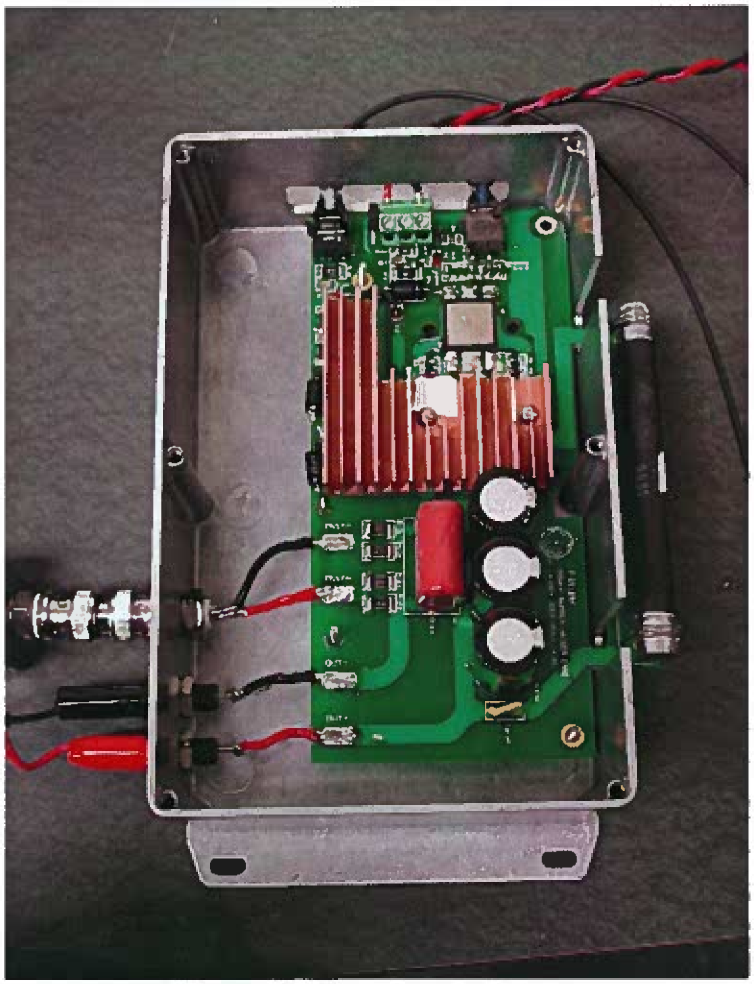


Figure 3. Power Supply Driver.

The circuit schematic is available in Appendix A.

3.1 Power Supply

The power supply driver provides a one-microsecond current pulse for the MOSFET boards' ferrite transformers at a set frequency. The MOSFET driver circuitry draws power from a separate 12V power supply while the medium voltage power supply (MVPS) on the output side is initially set to 20V multiplied by the number of boards that have to be powered. For eight 1kV MOSFET boards, the MVPS is initially set to 160V.

3.2 Operation

The output of the power supply driver is looped once through the eight ferrite cores of the MOSFET boards as, effectively, a single primary winding to the two secondary windings per core. As the power consumption demand of the 1kV boards increase, the frequency and amplitude of the current pulse must also be increased accordingly. At low frequencies, a current pulse at a frequency of 166kHz is sufficient to keep the MOSFET boards' supply voltage up to 16V. As the desired RFQ frequency increases, the current pulse frequency also must be increased to provide the boards sufficient power. Since the pulse is fixed at 1 microsecond, the current pulse frequency can only be increased to approximately 333kHz before the power transfer efficiency starts to decrease. In order to keep up with the power consumption needs, the MPVS voltage can also be increased beyond 20V per board. At an RFQ frequency of 2MHz, the medium voltage power supply should be set to 180V for an 8-board system. In order to run at 3MHz, the voltage should be increased even further to at least 200V, corresponding to 25V per board.

3.3 MOSFET Latch-up

Empirical observations have shown that if the gate of the MOSFET is driven high before there is a voltage applied across the drain and source, then the MOSFET has a tendency to latch up. In this state, the MOSFET will subsequently not switch on properly when a voltage is applied. This often occurs when the 12V power supply is turned on before the medium voltage power supply. In order to avoid this condition, the simplest method is to just turn on the medium voltage power supply before turning on the 12V power supply that powers the MOSFET driver. For additional redundancy, an interlock system has been implemented. A voltage transorb detects the voltage across the drain and source and sends a signal by an optical transmitter to the pulse controller board only when the voltage is sufficiently high. The pulse controller board waits for this signal before it starts switching the PSD.

3.4 Noise Considerations

In order to counter the effects of noise, low-pass filters with bandwidths of approximately 10MHz have been designed for the 12V and medium voltage power supply. However, the 12V power supply filter has LEMO connectors and the only way to adapt them to the PSD is to use adapter cables that add another 4m of wires to the circuit. This additional length adds 4V fluctuations to the power line, which is a significant amount of noise. Testing has shown that the system works fine without the 12V filter, so it has been left out altogether.

The MVPS filter originally used 12-inch cables to connect the different components of the filter but they have been replaced with adapters to reduce total wire length. All cables that cannot be shortened any further have been twisted into twisted pairs to attenuate EM pickup.

4.0 1kV Stack

The stack consists of eight 1kV boards, each of which contains a DE375-102N12A RF Power MOSFET used as a digital switch. Four boards connected such that the switches are in a series configuration form the pull-up network and the other four boards form the pull-down network. A resistance of 50 ohms put in series with the switches dampens oscillations caused by parasitic inductances in the circuit resonating with the capacitive load. The resistance can also act as a current-limiter should the pulse controller board malfunction and try to turn all 8 switches, thereby shorting the HVPS.

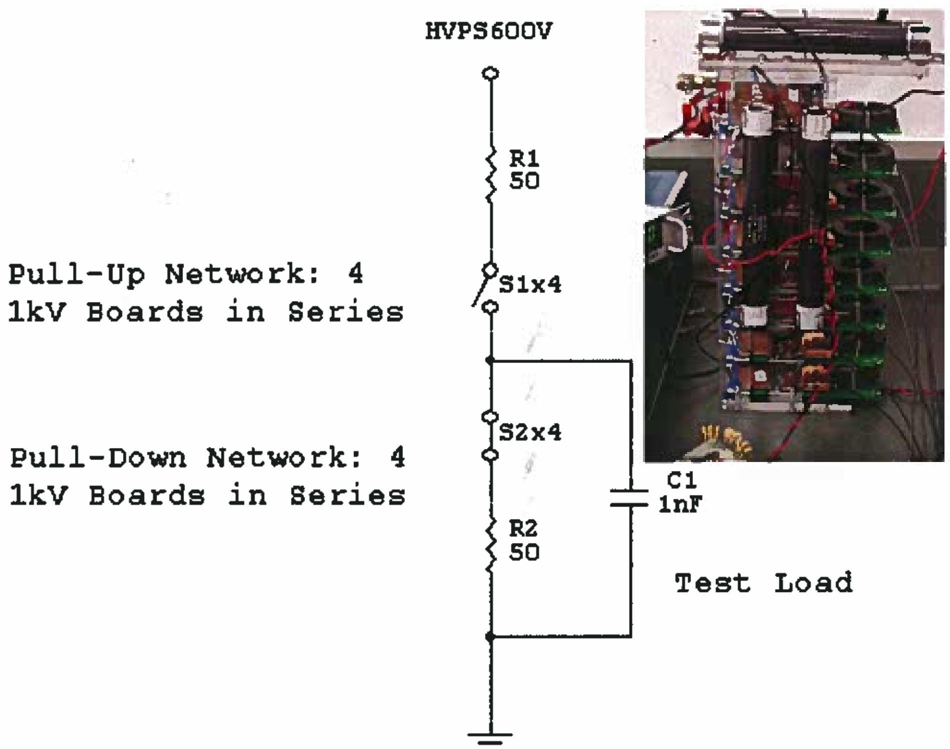


Figure 4. 1kV Stack Setup.

4.1 1kV Board

The figure on the next page shows the 1kV board with the heatsink and copper shield removed to expose the DE375-102N12A Power MOSFET and the DEIC420 MOSFET driver. The copper shield is fixed to the DEIC420 to act as a heatsink since the driver can source and sink a peak current of 20A. The shield also protects the fibre-optic receiver circuitry from EM interference so the input signal does not become corrupted.

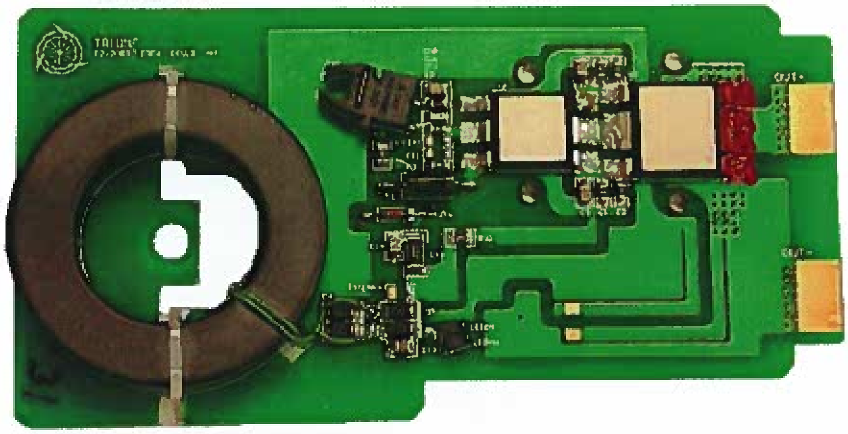


Figure 5. 1kV Board.

The board circuitry is powered with 16VDC supplied through a ferrite core transformer using pulsed power techniques. The most noteworthy component of which is the DEIC420 20 Ampere Low-Side Ultrafast RF MOSFET Driver that can be switched with a drive voltage anywhere between 8V and 30V. However, a 1V5KE18A Transient Voltage Suppressor prevents the drive voltage from rising above 18V.This is due to the fact that the DE375 has a maximum continuous V_{GS} rating of 20V. Limiting the voltage prevents the gate charge from punching through the insulator separating it from the substrate.

4.2 Stack Performance

At the time that this report was written, the only high voltage power supply available for testing of the MOSFET stack was a 600V 2A switched power supply. The following figure is a screenshot of the scope trace taken at 600V and 1.5MHz.

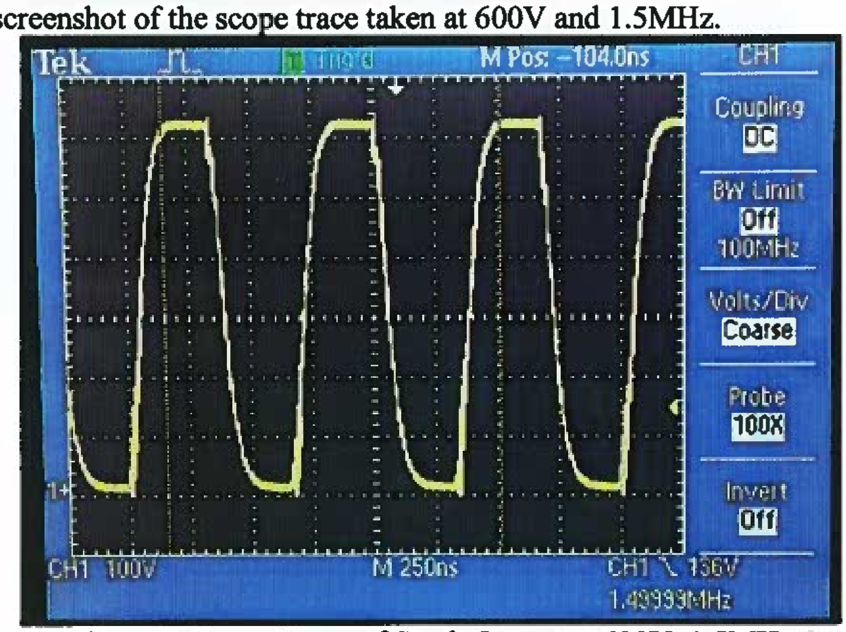


Figure 6. Scope Trace of Stack Output at 600V, 1.5MHz

The stack has been tested at up to 600V peak-to-peak at a frequency of 2.4MHz. The data relating power consumption of the MVPS and HVPS is presented below:

HVPS Voltage = 600V		R_{stack} = 50 ohms		R_{PSD} = 26 ohms	
RFQ Freq (kHz)	MVPS Current (A)	MVPS Voltage (V)	MVPS Power (W)	HVPS Current (A)	HVPS Power (W)
400	0.71	145	102.95	0.29	174
500	0.71	145	102.95	0.33	198
600	0.71	145	102.95	0.39	234
700	0.72	145	104.40	0.45	270
800	0.73	145	105.85	0.50	300
900	0.74	145	107.30	0.56	336
1000	0.76	145	110.20	0.61	366
1100	0.80	150	120.00	0.66	396
1200	0.82	150	123.00	0.72	432
1300	0.83	150	124.50	0.77	462
1400	0.84	150	126.00	0.83	498
1500	0.85	150	127.50	0.88	528
1600	0.93	160	148.80	0.94	564
1700	0.94	160	150.40	0.99	594
1800	0.95	160	152.00	1.04	624
1900	0.97	160	155.20	1.10	660
2000	0.98	160	156.80	1.16	696
2100	1.05	170	178.50	1.21	726
2200	1.06	170	180.20	1.28	768
2300	1.08	170	183.60	1.34	804
2400	1.10	170	187.00	1.39	834

Table 1. Power Consumption for $600V_{pp}$ Operation.

5.0 Heat Considerations

Due to the high power consumption of the system, a number of different components heat up during operation. It is therefore crucial to ensure that they do not heat up excessively and become damaged.

5.1 Power Resistors

The components that heat up the most are the power resistors in the switching loop and the PSD output loop. The resistors in the switch loop are 25 ohms each and, at $600V_{pp}$ and 2.4MHz, pass 1.39A of current. This corresponds to a power consumption of 48.3W, which is 25.4% of its maximum power rating. A heating curve obtained from the resistors' manufacturer, Kanthal Globar, indicates that the resistors should heat to 110°C above ambient temperature. Experiments have shown that the resistors heat to approximately 150°C, which is agreeable with an ambient temperature of 40°C.

The external PSD resistors are valued at 13 ohms and supply a maximum of 1.35A at a RFQ drive frequency of 3MHz. This corresponds to a power consumption of 23.7W and a theoretical rise of 60°C above ambient according to the heating curve. In reality, the temperature only rises by about 46°C to 86°C because of a Tarzan/Rotron TN3A2 85W fan that blows along the length of the resistor and through its hollow cylindrical hole. Since these type 886SP resistors can withstand up to 350°C, there should be no problem using them in this application.

5.2 Power MOSFETs

Another area of concern is the power MOSFETs. As the graph below indicates, current draw is linearly dependant on both RFQ frequency and peak-to-peak voltage.

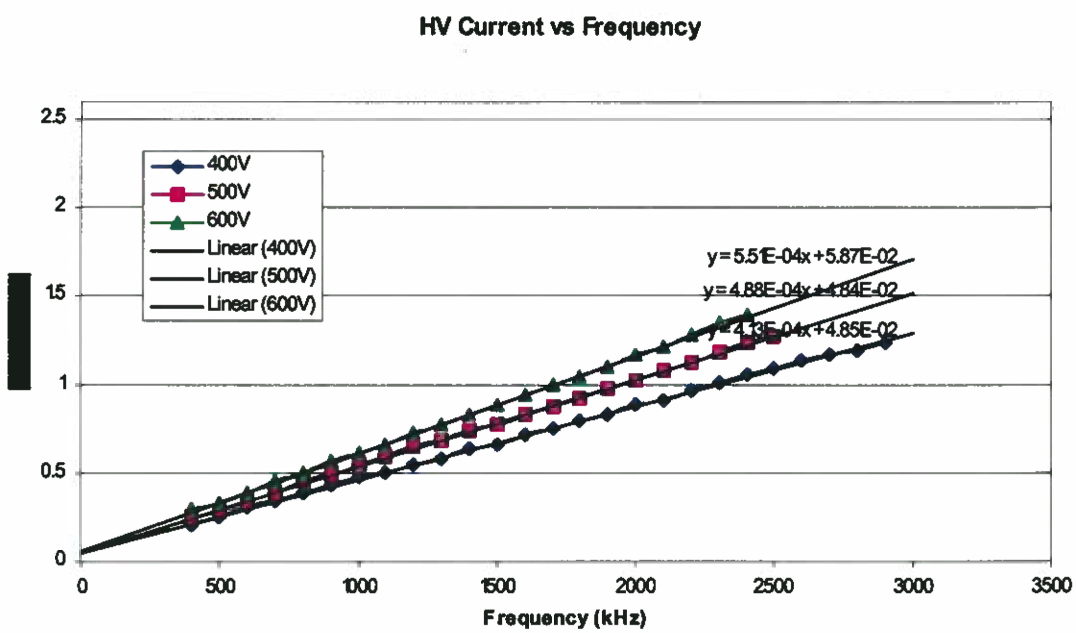


Figure 7. High Voltage Power Supply Current versus RFQ Frequency.

Currently, each transistor has a heatsink that increases its surface area to $210cm^2$. When the MOSFET is driving 1.35A of current, the heatsink only rises to 50.5°C. With the low power consumption of the MOSFET and a heatsink-to-junction thermal resistance of 0.35°C/W, the junction temperature should be no higher than 52°C, well below the tolerance level of 175°C. Since one of the design goals in developing the RFQ electronics system is also to conserve space, it is also possible to reduce the height of the heatsinks, allowing the stack structure that houses the boards to be shortened.

5.3 Load Capacitor

The load capacitor used to simulate the quadrupoles had been noted to heat up to over 100°C. The original capacitor used for this application was a type Z5U DC capacitor. As the figure shows, the dielectric constant, and hence the capacitance, changes greatly with respect to temperature for the Z5U-type capacitor. As the temperature increases, the capacitances decrease drastically.

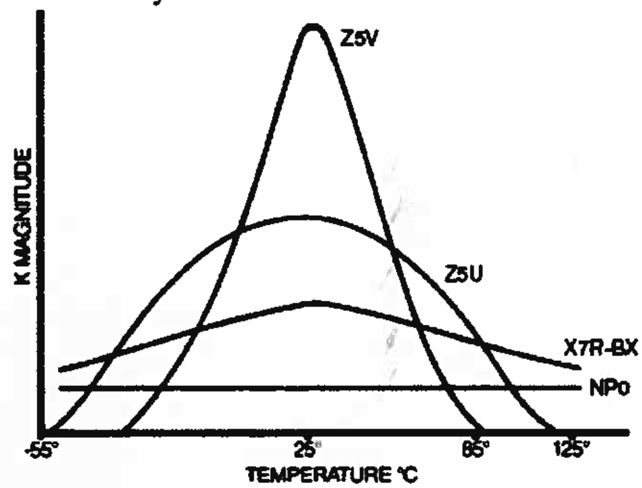


Figure 8. Changes in dielectric constant (K) with temperature for various ceramic dielectrics. [2]

This reduced capacitance meant that the square waveform exhibited oscillations characteristic of an under-damped system. Also, the HVPS was not supplying as much current as it should. This capacitor was replaced with a 2x2 array of AC capacitors that were less temperature-dependent. The new load behaved much more in accordance with theoretical values.

6.0 Timing Considerations

Compared to Dr. Michael J. Barnes' 25-kV 75-kHz kicker for measurement of muon lifetime, relatively, the RFQ driver has a longer rise-time and fall-time due to the higher load capacitance. The 25-kV 75-kHz kicker has a 40ns 10-to-90% rise-time while the RFQ driver has a 90ns rise-time [1]. As such, MOSFET switching delay timing considerations are not as important for the RFQ driver: Not only is the slew-rate lower, but the voltage across each board is also less.

Nevertheless, in order to reduce excess power dissipation, the boards' turn-on delays have been matched to within one nanosecond of each other. By taking initial measurements of the boards' delays, it was possible to determine the additional delay needed for each board. A simple R-C network provided additional delay by using the following formula:

$$C_{11} = \frac{\text{delay (in ns)}}{(0.9 * 680\Omega)}.$$

The table in Appendix B illustrates this process. Capacitors are picked by hand and soldered. As a result, all boards switch at approximately the same time within 1 nanosecond of each other.

7.0 System Performance

Currently, the stack can switch at over 2MHz at $600V_{pp}$. By reducing the voltage to $500V_{pp}$, 3MHz operation can be achieved. The following tables present the current operational limits of the RFQ driver system.

7.1 $400V_{pp}$

HVPS Voltage: 400V			R_{stack} = 50 ohms			R_{PSD} = 26 ohms		
Pot Setting	RFQ Frequency	MVPS Current	MVPS Voltage	MVPS Power	HVPS Current	HVPS Power	HVPS Theoretical Current	Actual-to-Theoretical Current Ratio
	kHz	A	V	W	A	W	A	
F	400	0.72	145	104.40	0.20	80	0.16	1.25
F	500	0.72	145	104.40	0.25	100	0.20	1.25
F	600	0.72	145	104.40	0.30	120	0.24	1.25
F	700	0.73	145	105.85	0.34	136	0.28	1.21
F	800	0.74	145	107.30	0.38	152	0.32	1.19
F	900	0.75	145	108.75	0.43	172	0.36	1.19
F	1000	0.76	145	110.20	0.47	188	0.40	1.18
F	1100	0.77	145	111.65	0.50	200	0.44	1.14
F	1200	0.78	145	113.10	0.54	216	0.48	1.13
F	1300	0.79	145	114.55	0.58	232	0.52	1.12
F	1400	0.84	150	126.00	0.63	252	0.56	1.13
F	1500	0.85	150	127.50	0.66	264	0.60	1.10
F	1600	0.86	150	129.00	0.71	284	0.64	1.11
F	1700	0.95	160	152.00	0.75	300	0.68	1.10
F	1800	0.95	160	152.00	0.79	316	0.72	1.10
F	1900	0.97	160	155.20	0.83	332	0.76	1.09
F	2000	0.98	160	156.80	0.88	352	0.80	1.10
F	2100	1.05	170	178.50	0.91	364	0.84	1.08
F	2200	1.06	170	180.20	0.96	384	0.88	1.09
F	2300	1.08	170	183.60	1.01	404	0.92	1.10
F	2400	1.10	170	187.00	1.05	420	0.96	1.09
F	2500	1.18	180	212.40	1.09	436	1.00	1.09
F	2600	1.18	180	212.40	1.13	452	1.04	1.09
F	2700	1.19	180	214.20	1.16	464	1.08	1.07
F	2800	1.28	190	243.20	1.19	476	1.12	1.06
F	2900	1.29	190	245.10	1.23	492	1.16	1.06
F	3000	1.35	200	270.00	1.26	504	1.20	1.05

Table 2. Data for $400V_{pp}$ Operation.

The current ratio represents how closely the HVPS output current agrees with the theoretical values for a 1nF capacitance load. The theoretical value only takes into account the load capacitance, ignoring any capacitance in the rest of the circuit, such as the MOSFETs' input capacitance.

7.2 500V_{pp}

HVPS Voltage: 500V			R_{stack} = 50 ohms			R_{PSD} = 26 ohms		
Pot Setting	RFQ Frequency	MVPS Current	MVPS Voltage	MVPS Power	HVPS Current	HVPS Power	HVPS Theoretical Current	Actual-to-Theoretical Current Ratio
	kHz	A	V	W	A	W	A	
F	400	0.72	145	104.40	0.25	150	0.20	1.25
F	500	0.72	145	104.40	0.28	168	0.25	1.12
F	600	0.72	145	104.40	0.34	204	0.30	1.13
F	700	0.73	145	105.85	0.39	234	0.35	1.11
F	800	0.74	145	107.30	0.45	270	0.40	1.13
F	900	0.75	145	108.75	0.49	294	0.45	1.09
F	1000	0.76	145	110.20	0.54	324	0.50	1.08
F	1100	0.81	150	121.50	0.59	354	0.55	1.07
F	1200	0.82	150	123.00	0.64	384	0.60	1.07
F	1300	0.83	150	124.50	0.68	408	0.65	1.05
F	1400	0.85	150	127.50	0.73	438	0.70	1.04
F	1500	0.86	150	129.00	0.77	462	0.75	1.03
F	1600	0.94	160	150.40	0.83	498	0.80	1.04
F	1700	0.95	160	152.00	0.87	522	0.85	1.02
F	1800	0.96	160	153.60	0.92	552	0.90	1.02
F	1900	1.04	170	176.80	0.97	582	0.95	1.02
F	2000	1.05	170	178.50	1.02	612	1.00	1.02
F	2100	1.06	170	180.20	1.07	642	1.05	1.02
F	2200	1.07	170	181.90	1.12	672	1.10	1.02
F	2300	1.08	170	183.60	1.18	708	1.15	1.03
F	2400	1.10	170	187.00	1.23	738	1.20	1.03
F	2500	1.10	170	187.00	1.27	762	1.25	1.02
F	2600	1.32	200	264.00	1.32	792	1.30	1.02
F	2700	1.35	200	266.00	1.35	810	1.35	1.00
F	2800	1.40	200	268.00	1.40	840	1.40	1.00
F	2900	1.45	200	272.00	1.45	870	1.45	1.00
F	3000	1.50	200	274.00	1.50	900	1.50	1.00

Table 3. Data for 500V_{pp} Operation.

7.3 600V_{pp}

HVPS Voltage: 600V			R_{stack} = 50 ohms			R_{PSD} = 26 ohms		
Pot Setting	RFQ Frequency	MVPS Current	MVPS Voltage	MVPS Power	HVPS Current	HVPS Power	HVPS Theoretical Current	Actual-to-Theoretical Current Ratio
	kHz	A	V	W	A	W	A	
F	400	0.71	145	102.95	0.29	174	0.24	1.21
F	500	0.71	145	102.95	0.33	198	0.30	1.10
F	600	0.71	145	102.95	0.39	234	0.36	1.08
F	700	0.72	145	104.40	0.45	270	0.42	1.07
F	800	0.73	145	105.85	0.50	300	0.48	1.04
F	900	0.74	145	107.30	0.56	336	0.54	1.04
F	1000	0.76	145	110.20	0.61	366	0.60	1.02
F	1100	0.80	150	120.00	0.66	396	0.66	1.00
F	1200	0.82	150	123.00	0.72	432	0.72	1.00
F	1300	0.83	150	124.50	0.77	462	0.78	0.99
F	1400	0.84	150	126.00	0.83	498	0.84	0.99
F	1500	0.85	150	127.50	0.88	528	0.90	0.98
F	1600	0.93	160	148.80	0.94	564	0.96	0.98
F	1700	0.94	160	150.40	0.99	594	1.02	0.97
F	1800	0.95	160	152.00	1.04	624	1.08	0.96
F	1900	0.97	160	155.20	1.10	660	1.14	0.96
F	2000	0.98	160	156.80	1.16	696	1.20	0.97
F	2100	1.05	170	178.50	1.21	726	1.26	0.96
F	2200	1.06	170	180.20	1.28	768	1.32	0.97
F	2300	1.08	170	183.60	1.34	804	1.38	0.97
F	2400	1.10	170	187.00	1.39	834	1.44	0.97

Table 4. Data for 600V_{pp} Operation.

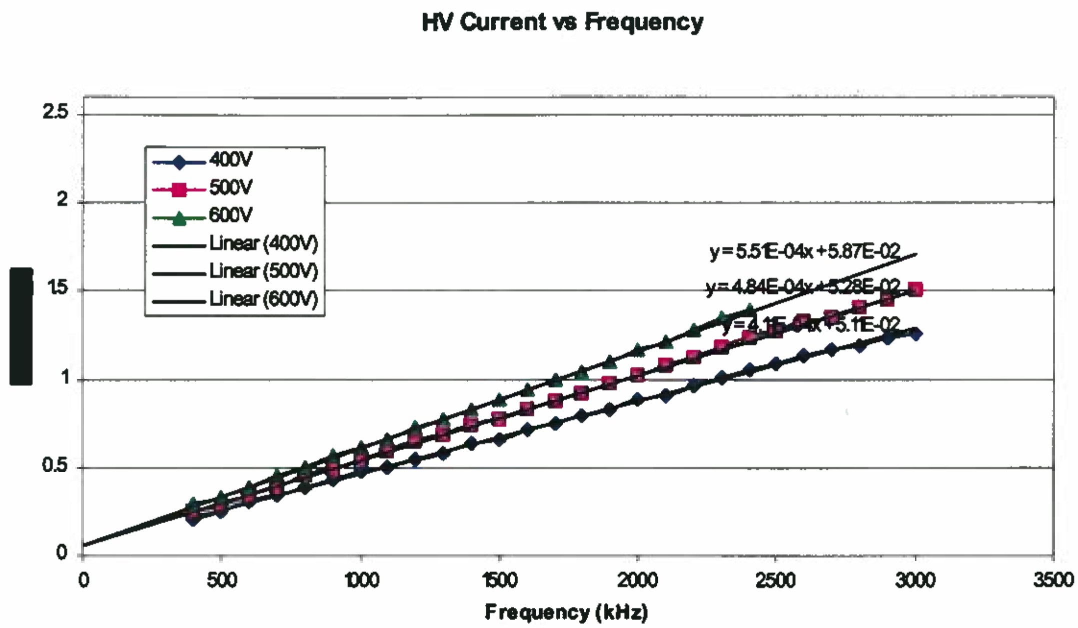


Figure 6. High Voltage Power Supply Current versus RFQ Frequency.

As evident, both the MPVS and HVPS power consumption scale approximately linearly with RFQ frequency as well as voltage. It can be estimated that when the system runs at $1000V_{pp}$ and 3MHz, the current consumption should be approximately 3A.

When the stack is switching $600V_{pp}$, the output waveform tends to break down at frequencies above 2.2MHz. The stack would stop switching for approximately half a millisecond before starting up again. This phenomenon becomes more frequent as the frequency increases and is easy to detect because the current consumed by the system begins to decline significantly with RFQ frequency.

An attempt was made to switch only six MOSFET boards instead of eight, taking out two boards. This resulted in a maximum operational frequency of only 1.89MHz at 600V peak-to-peak. This supports the conclusion that the higher the applied V_{GS}, the lower the maximum operational frequency, since now 600V is being distributed across 3 boards instead of 4.

8.0 Conclusion and Recommendations

Currently, the RFQ driver can achieve $600V_{pp}$ 2.2MHz. At 3MHz, the RFQ driver can switch up to $500V_{pp}$ before it begins to stall. The MOSFET switches have problems switching at high (2.2MHz and above) frequencies, depending on the voltage being applied across the drain and source. As the applied voltage increases, the maximum achievable switching frequency decreases. One way to achieve higher voltage should be possible by adding more 1kV boards, perhaps upgrading the stack to a 5-up 5-down or 6-up 6-down configuration.

The current setup keeps all power components, including MOSFETs and heat sinks, well below their tolerable temperature limits. Should the need to reduce space arrive, the MOSFET heatsinks can be reduced in height from 1" to ½", thereby reducing the total stack height. The ceramic tubular 190W resistors can be replaced with ones of lower power rating, such as the 150W or 90W ones, which are proportionally smaller.

The RFQ driver at its current state should have no problem confining and focusing heavier ion beams. At 400V 3MHz, the lowest acceptance voltage, ions of mass 4 can be confined. Since the stack has not been tested at its upper operational limits, the RFQ driver may have problems accepting and focusing a large number of lighter ions. There are no foreseen problems with replacing the test load capacitor with the actual RFQ, but that remains to be seen.

The RFQ capacitance should be minimized to reduce power consumption by reducing current draw from the HVPS. When the MOSFETs are switching high currents, they are put under a lot of strain due to increased heating of the transistor junction. A lower load capacitance would decrease the current draw, subsequently causing less heat dissipation.

References

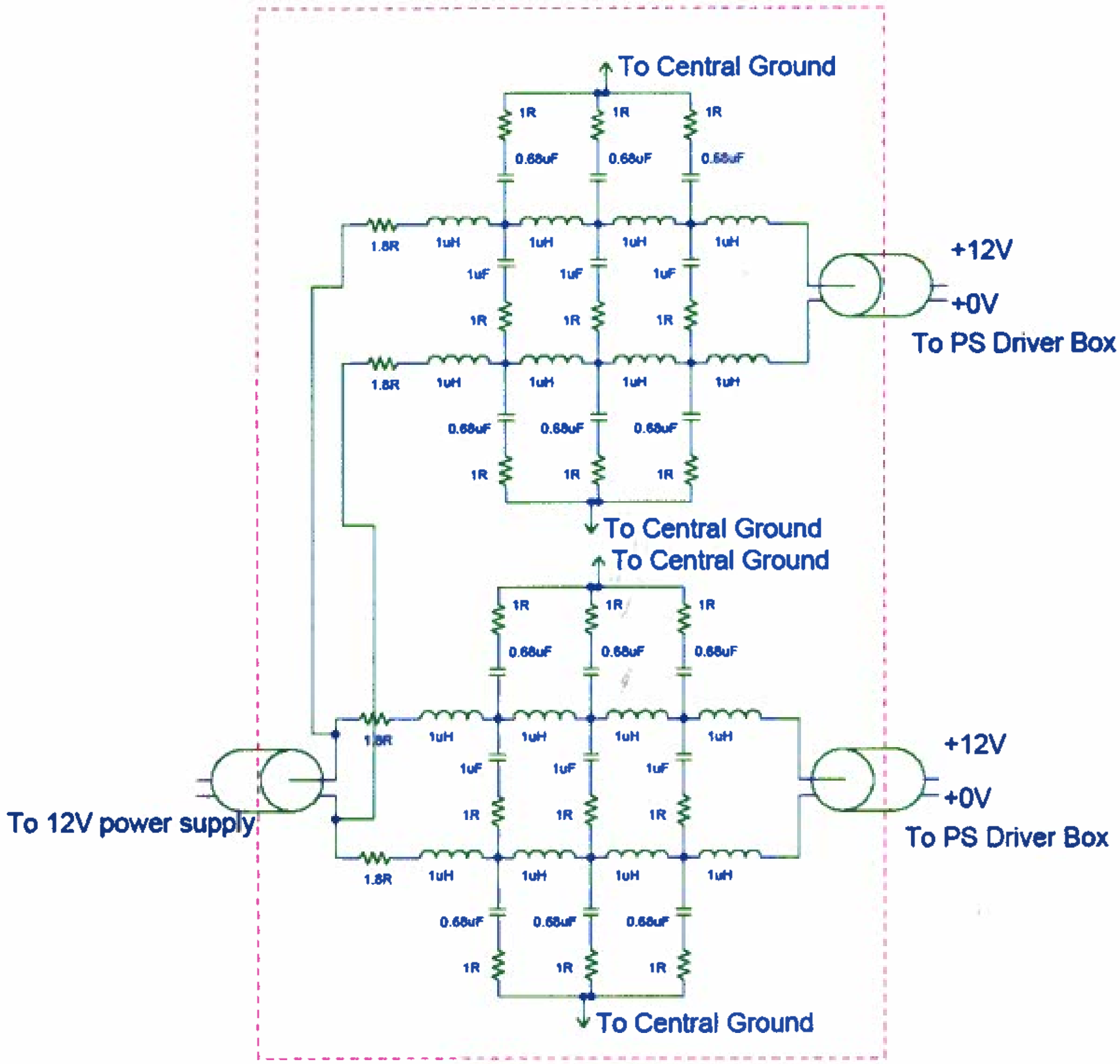
[1] M. J. Barnes and G. D. Wait, "Design for a FET based 1 MHz, 10kV pulse generator," in IEEE Transactions on Plasma Science, Vol. 32, No. 5, October 2004, p. 1942.

[2] Kahn, Manfred, "Technical Information: Multi-layer Ceramic Capacitors – Materials and Manufacture." April 5, 2005. <http://www.avxcorp.com/docs/techinfo/mlcmat.pdf>

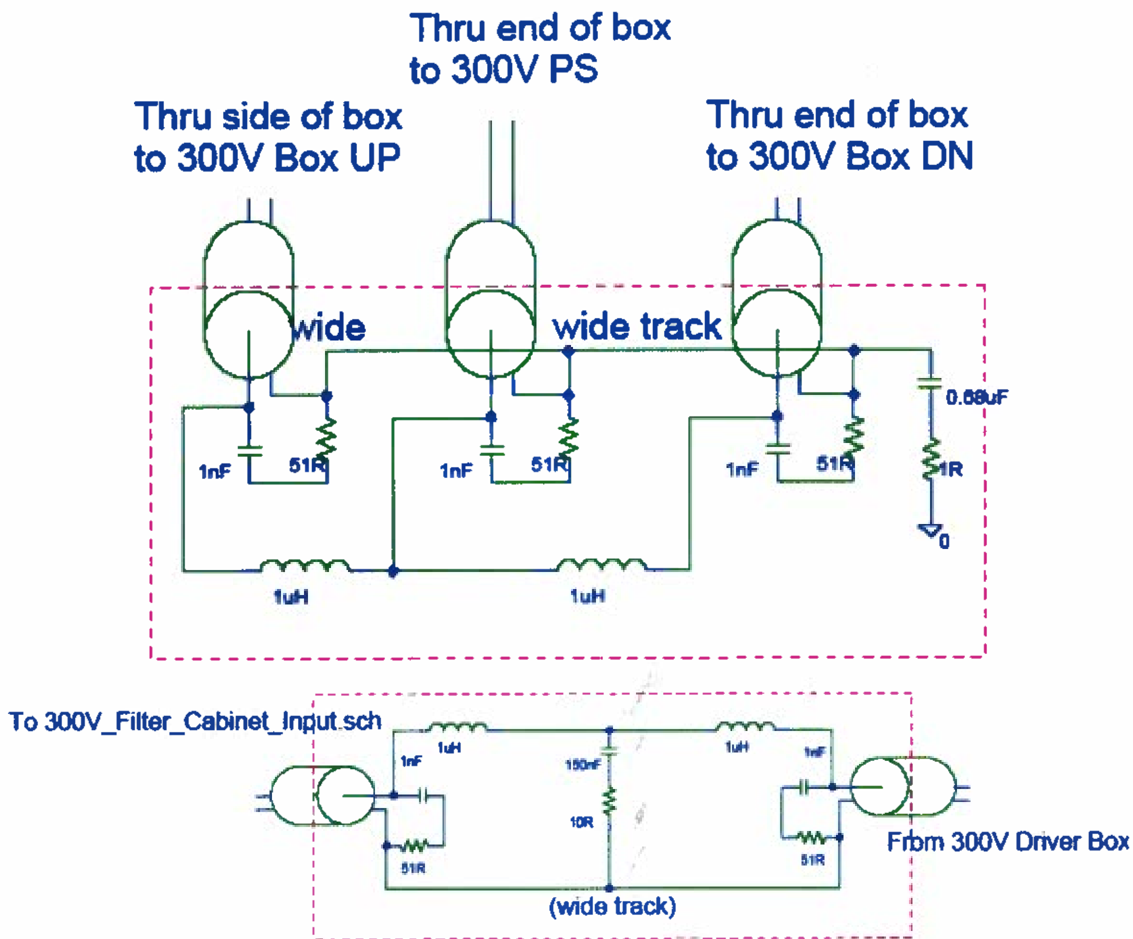
[3] TITAN website, "RFQ Ion Trap: PowerPoint presentation", 18 Dec. 2003. <http://www.triumf.ca/titan>

Appendix A – Circuit Diagrams

12V Power Supply Filter

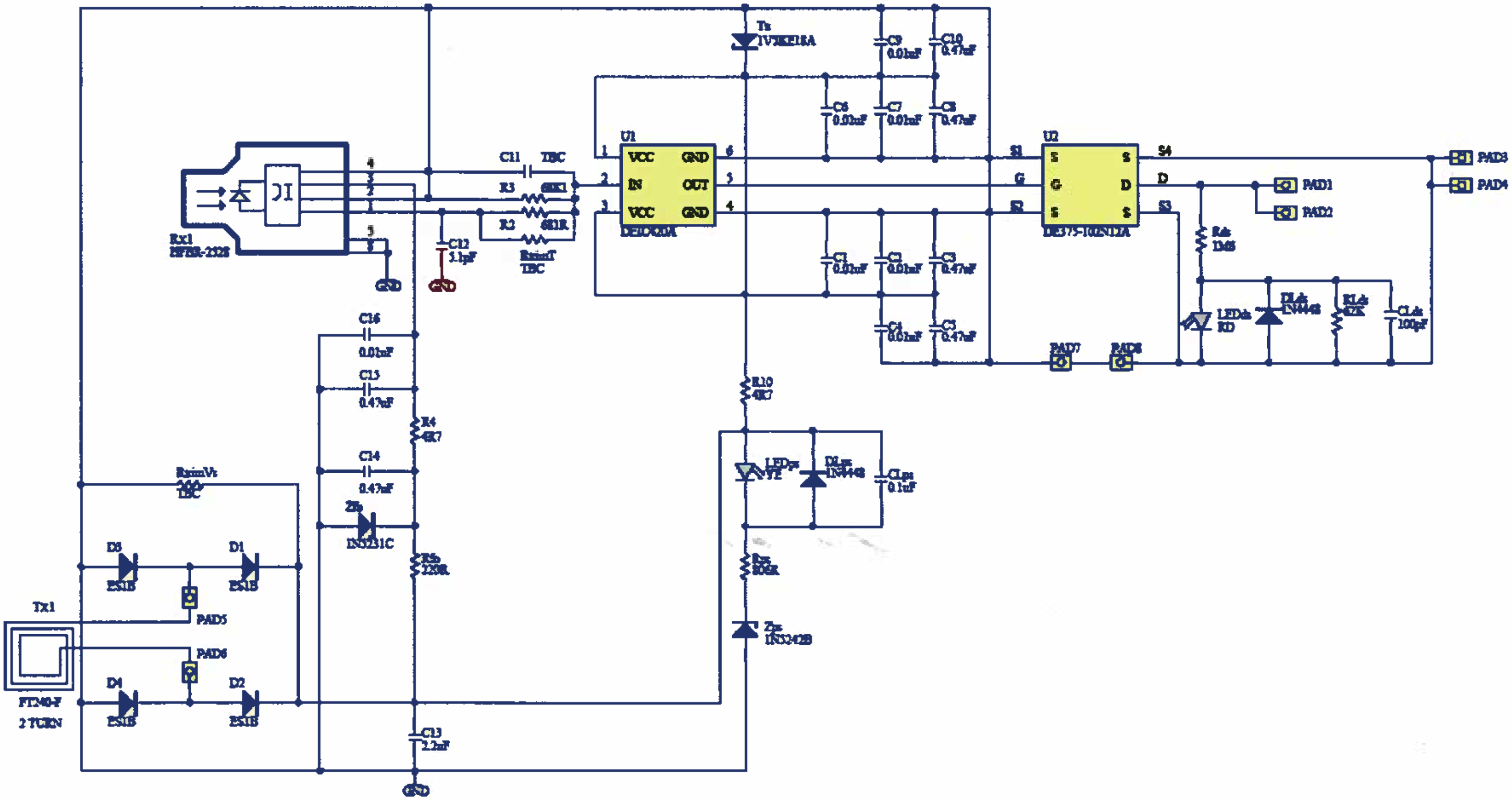


300V Power Supply Filter *



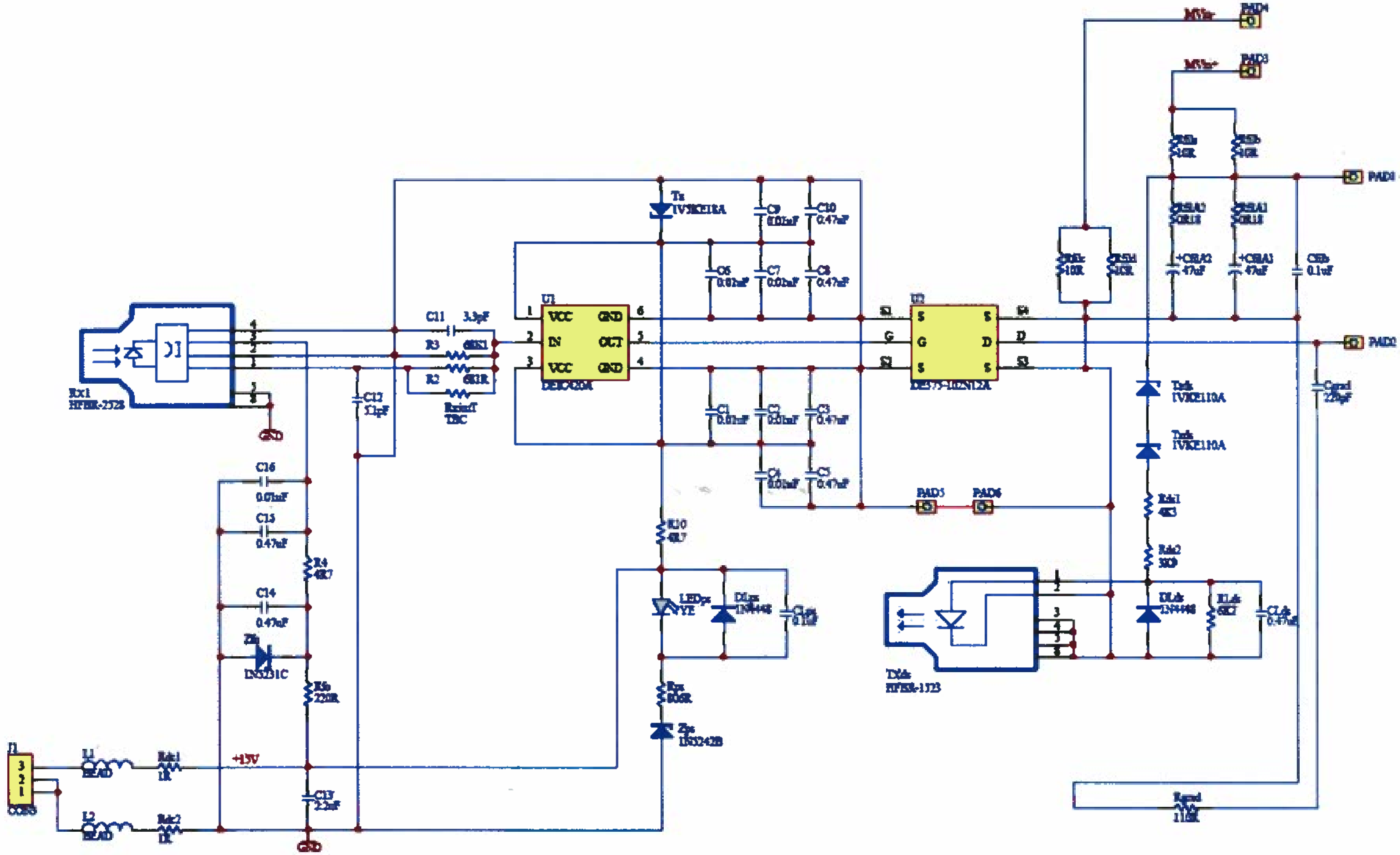
*"To 300V_Filter_Cabinet_Input.sch" connects to either "Thru side of box to 300V Box UP" or "Thru end of box to 300V Box DN."

1kV Board



U1
VCC
IN
GND
OUT
U2
S
G
D
S1
S2
S3
S4
PAD1
PAD2
PAD3
PAD4
PAD5
PAD6
PAD7
PAD8
Rx1
C11
TBC
R3
R2
C12
5.1pF
GND
C16
0.01uF
C13
0.47uF
R4
4R7
C14
1N5231C
220R
R10
4R7
D1
D2
D3
D4
ES1B
Tx1
FT240-F
2 TURN
1N4448
0.1uF
100pF
1M8

Power Supply Driver Circuit



Appendix B – Timing Table

Board #	C13 Voltage (V)	MPVS Current (A)	Pull-Down Delay (ns)	Delay to be Added (ns)	C11 Value (pF)	C11 - Theoretical (pF)	C11 - Used (pF)	Final Delay (ns)
20	15.55	0.20	260	12	19.6	20	20	272
21	15.70	0.20	258	14	22.9	22+1	22	272
22	15.41	0.20	262	10	16.3	15+1	15	272
23	15.38	0.21	264	8	13.1	12+1	12	272
24	15.88	0.20	262	10	16.3	15+1	15	274
25	15.60	0.20	268	4	6.5	6.8	5.1	272
26	15.42	0.21	260	12	19.6	20	20	272
27	15.60	0.20	260	12	19.6	20	20	274
28	15.82	0.20	256	16	26.1	22+3.9	22	274
29	15.83	0.20	262	10	16.3	15+1	15	274
30	15.82	0.20	270	2	3.3	3.3	1	274
31	16.01	0.21	266	6	9.8	10	0	274
Others			272					

Data for matching new 1kV boards to existing 1kV boards.

Boards #20-31 are the new 1kV boards made after January 1st, 2005. Their timing characteristics have been matched to the first stack of 1kV boards.

Appendix C – Instruction for Operation

Turning on the Stack

1. Turn on signal generator supply drive frequency. Set amplitude to $2.5V_{pp}$ square wave, offset to $1.25V_{DC}$, and frequency to 1MHz.

2. Turn on 5V power supply for the pulse controller board, 12V power supply for the power supply driver, and power on the medium voltage power supply and high voltage power supply.

3. Increase the medium voltage power supply voltage to 20V multiplied by the number of MOSFET boards.

4. Increase the high voltage power supply voltage to the desired drive voltage.

5. Increase the signal generator frequency to the desired drive frequency, while increasing the medium voltage power supply voltage according to the table, ensuring that the onboard LEDs on the 1kV boards do not become dim.

Turning off the Stack

1. Decrease the signal generator frequency to 1MHz, while decreasing the medium voltage power supply voltage according to the table, ensuring that the onboard LEDs on the 1kV boards do not become too bright.

2. Decrease the high voltage power supply voltage to 0.

3. Decrease the medium voltage power supply voltage to 0. Trigger board should stop switching due to activation of MV Interlock.

4. Turn off all power supplies.