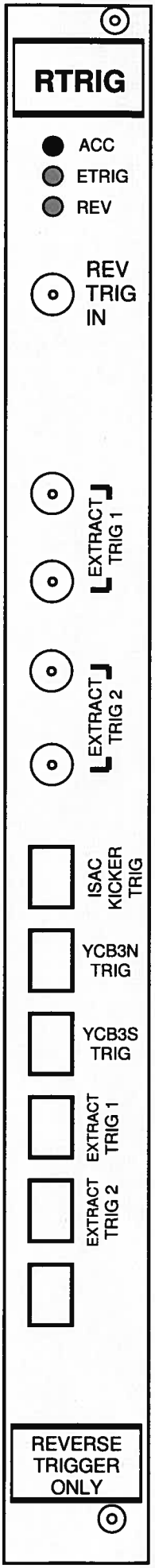


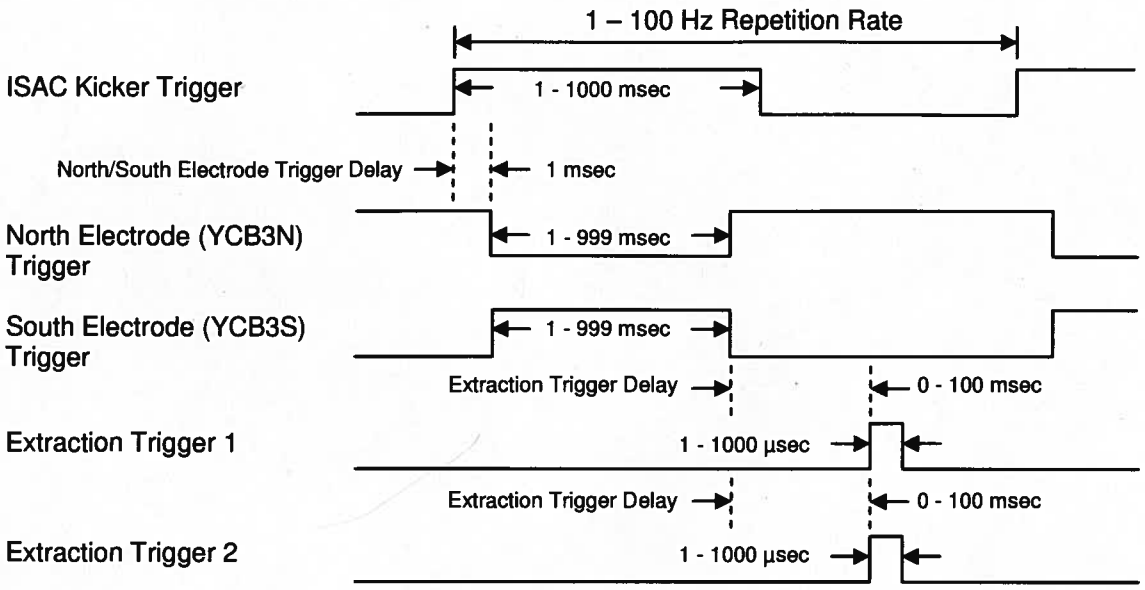
TRIUMF

TITAN VME Reverse Trigger Module

General Description

The VME Reverse Trigger Module (RTRIG) was designed to generate the following gate pulses.

Reverse Extraction



Once the RTRIG module detects a trigger pulse, the waveforms as described above will be generated. If a second main trigger pulse is injected before the **ISAC kicker trigger** pulse finishes, it is ignored.

VME Interface

SLAVE – A16, D16, D8 (OE)

The RTRIG requires a 16-bit address space. Jumpers on the printed circuit board configure the base address selection.

Address Modifier Selection

The RTRIG will only respond to A16 address cycles.
Short Supervisory & short nonprivileged access - 0x2D, 0x29